Collected LWA Engineering Memos
From the Development of the Analog Signal Processor (ASP)

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Editor: Jayce Dowell (UNM)

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LWA Engineering Memo

Analog Signal Path GNI and ARX Block Diagam v.1

Task: ARX0003
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April 11, 2008

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1. Analog Signal Path Background and Requirements

The analog signal path is defined as the input to the front-end electronics through the output of the analog receiver and contains the Front-End Electronics (FEE), RF and Power Distribution (RPD), Shelter Entry Panel (SEP), and the Analog Receiver (ARX) as shown in Figure 1. In order to optimally digitize the signals which exists at the antenna terminals, proper design of the gain, linearity and noise figure in the analog signal path is crucial. This report discusses the current state of the analog signal path, presents a preliminary block diagram of the ARX and analyzes the impact of the design options on the GNI of the analog signal path.

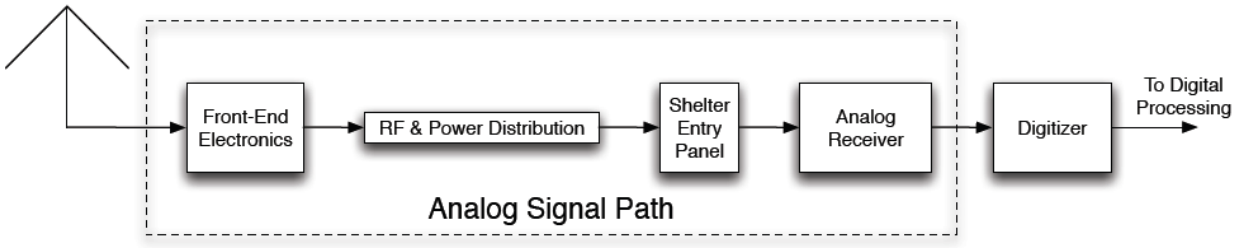

Figure 1: LWA Analog Signal Path

A summary of the analog signal path GNI requirements from LWA Memo 121 are as follows:

1) The total gain of the analog signal path should be variable over the range of 37dB to 82dB (although 47-77dB is probably sufficient).
2) The entire analog signal path should maintain a noise temperature close to that of the FEE chosen.
3) The analog signal path should have a total IIP3 of -22dBm or better when using minimum gain.

LWA Memo 121 (table 9) provides an initial GNI analysis of the analog signal path. Due to the unreasonable requirements placed on the ARX stage by FEE options "Hicks" (LWA Memo 19) and "RTA+" (LWA Memo 120, modified by changing the final gain stage to a GALI-74 to increase gain); these FEEs will not be discussed in this report. This document presents an ARX design for the analog signal path with FEE options "RTA" (LWA Memo 120, modified to insert BPF between gain stages) and "120K" active-balun (LWA Memo 81).

2. **ARX Requirements**

Assuming 15dB of loss for 150m RG-58 at 38MHz and ignoring any additional losses from SEP, etc., we can derive a set of requirements (Table 1) for the ARX based on the two FEEs and the required GNI of the analog signal path above [1].

FEE	ARX Min. Gain	ARX Max. Gain	NF	IIP3 @ Max. Gain
RTA	17dB	62dB	7dB	-2dBm
120K	20dB	65dB	7dB	-5dBm

Table 1: ARX required Gain, Noise Figure and Linearity for the two candidate FEEs

The required metrics for these two FEEs are close enough to be viewed as identical, therefore, the analysis will now only focus on the RTA balun because the two baluns are interchangable and only affect the final system temperature.

3. **ARX Block Diagram and GNI**

The block diagram in Figure 2 was generated using actual components available to achieve the ARX GNI requirements stated above. The coax relay is used as input protection. The design detail of the filters are not covered in this report, although an insertion loss of 1.5dB is assumed through each filter. All amplifiers are Minicircuits' Gali-74. The step attenuators are Minicircuits' DAT-31 digital step attenuators. The RF switches are M/A Com's SS0192 switch. These may not be the final components selected, but are a good representation of what is available. For reference, the PAPER telescope's analog receiver amplifiers are Hittite's HMC476MP86 [3]. This amplifier was discarded due to it's poor linearity (IIP3 = +5dBm). Another amplifier, Minicircuits Hela-74 has extremely good linearity (IIP3 = +37dBm), but was discarded because of it's high price and extremely high current draw (500mA).

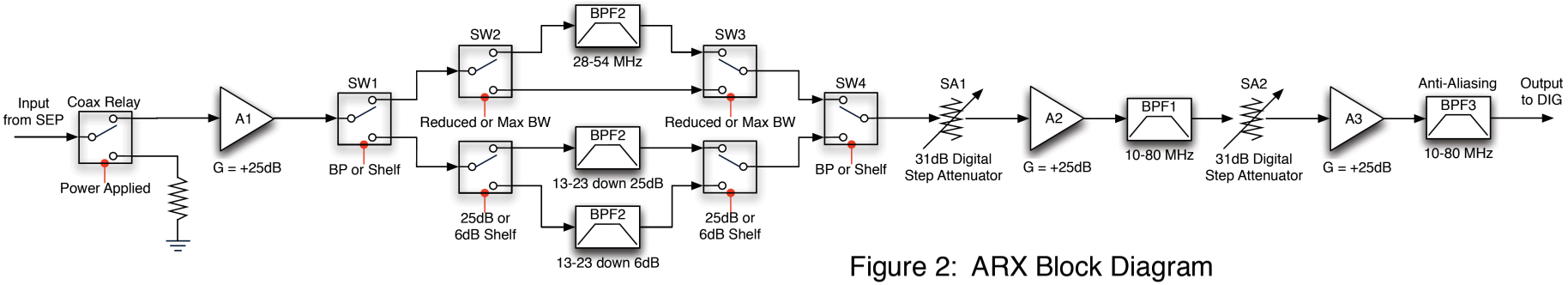

Figure 2: ARX Block Diagram

Max. Gain (G = +62dB)	Stage Characteristic			ARX Characteristic		
Component	**Gain [dB]**	**NF [dB]**	**IIP3 [dBm]**	**Gain [dB]**	**NF [dB]**	**IIP3 [dBm]**
Coaxial Relay	-1.0	1.0	200.0	-1.0	1.0	200.0
A1 - Gali74	25.1	2.7	12.9	24.1	3.7	13.9
SW1 - S0192	0.2	0.2	53.0	23.9	3.7	13.8
SW2 - S0192	0.2	0.2	53.0	23.7	3.7	13.8
BPF1	-1.5	1.5	200.0	22.2	3.7	13.8
SW3 - S0192	0.2	0.2	53.0	22.0	3.7	13.7
SW4 - S0192	0.2	0.2	53.0	21.8	3.7	13.7
SA1 - DAT31	-5.3	5.3	52.0	16.5	3.7	13.6
A2 - Gali74	25.1	2.7	12.9	41.6	3.8	-3.7
BPF2	-1.5	1.5	200.0	40.1	3.8	-3.7
SA2 - DAT31	-1.3	1.3	52.0	38.8	3.8	-3.8
A3 - Gali74	25.1	2.7	12.9	63.9	3.8	-25.9
BPF3	-1.5	1.5	200.0	**62.4**	**3.8**	**-25.9**

Max. Gain Configuration	Stage Characteristic			System Characteristic		
Stage	**Gain [dB]**	**NF [dB]**	**IIP3 [dBm]**	**Gain [dB]**	**NF [dB]**	**IIP3 [dBm]**
FEE - RTA	35.0	2.7	-2.3	35.0	2.7	-2.3
RPD - RG58	-15.0	15.0	200.0	20.0	2.7	-2.3
ARX	**62.4**	**3.8**	**-25.9**	**82.4**	**2.8**	**-45.9**

Table 2: ARX GNI & Analog Signal Path GNI for the Maximum Gain Configuration

Min. Gain (G = +17dB)	Stage Characteristic			ARX Characteristic		
Component	**Gain [dB]**	**NF [dB]**	**IIP3 [dBm]**	**Gain [dB]**	**NF [dB]**	**IIP3 [dBm]**
Coaxial Relay	-1.0	1.0	200.0	-1.0	1.0	200.0
A1 - Gali74	25.1	2.7	12.9	24.1	3.7	13.9
SW1 - S0192	0.2	0.2	53.0	23.9	3.7	13.8
SW2 - S0192	0.2	0.2	53.0	23.7	3.7	13.8
BPF1	-1.5	1.5	200.0	22.2	3.7	13.8
SW3 - S0192	0.2	0.2	53.0	22.0	3.7	13.7
SW4 - S0192	0.2	0.2	53.0	21.8	3.7	13.7
SA1 - DAT31	-19.3	19.3	52.0	2.5	4.6	13.6
A2 - Gali74	25.1	2.7	12.9	27.6	5.3	8.7
BPF2	-1.5	1.5	200.0	26.1	5.3	8.7
SA2 - DAT31	-32.3	32.3	52.0	-6.2	8.8	8.6
A3 - Gali74	25.1	2.7	12.9	18.9	10.5	8.2
BPF3	-1.5	1.5	200.0	**17.4**	**10.5**	**8.2**

Min. Gain Configuration	Stage Characteristic			System Characteristic		
Stage	**Gain [dB]**	**NF [dB]**	**IIP3 [dBm]**	**Gain [dB]**	**NF [dB]**	**IIP3 [dBm]**
FEE - RTA	35.0	2.7	-2.3	35.0	2.7	-2.3
RPD - RG58	-15.0	15.0	200.0	20.0	2.7	-2.3
ARX	**17.4**	**10.5**	**8.2**	**37.4**	**3.0**	**-12.3**

Table 3: ARX GNI & Analog Signal Path GNI for the Minimum Gain Configuration

The key to this design is in the ability to achieve a decent noise figure at low gains and a decent IIP3 at high gain. This architecture and subsequent GNI analysis assumes SA1 is set to 4dB attenuation and SA2 is set to 0dB attenuation for maximum ARX gain; while SA1 is set to 18dB attenuation and SA2 is set to 31dB attenuation for minimum ARX gain. The architecture provides enough isolation between amplifiers, decent noise figure and moderate IIP3 throughout the gain control range. The advantage of placing the attenuators at different cascaded locations is to provide the system another parameter of configurability; balancing receiver linearity, gain, and noise figure. For example, a higher noise figure may be preferred over a decrease in linearity, in which case, setting SA1's attenuation before SA2's attenuation would be implemented.

Tables 2 and 3 show the ARX GNI analysis and the analog signal path GNI with the maximum and minimum gain configurations. The ARX characteristics are used as the ARX stage characteristics in the system analysis. The maximum gain configuration (+82dB) is used when a maximum signal level of -89dBm is present (Pclip = +3dBm with 10dB of margin, Pmax = -7dBm). Taking P1dB to be 10dB higher, P1dB should be -79dBm. Taking IIP3 to be 15dB higher, IIP3 should be -64dBm. The predicted IIP3 of the system in max. gain configuration is -46dBm. The minimum gain configuration (+37dB) is used when a maximum signal level of -44dBm is present. Taking P1dB to be 10dB higher, P1dB should be -34dBm. Taking IIP3 to be 15dB higher, IIP3 should be -19dBm. The predicted IIP3 of the system in min. gain configuration is -12dBm. Of course many gain configurations exist between the max. and min. configurations that will yield comparable noise figure and linearity performance.

The reconfigurable filters may not be implemented with a switched filter bank as in Figure 2. Instead, a diplexer, attenuator and combiner architecture may provide better selectivity performance. It is assumed that the diplexer configuration will not change the GNI significantly, therefore, the results of the switched filter bank configuration holds true for the diplexer configuration also.

4. **RPD Considerations**

The RPD (aka cabling) will not only attenuate the signal from FEE to ARX significantly, but will attenuate higher frequencies more than lower frequencies. Also, if the cable lengths from antenna to shelter are not uniform, the loss in the RPD will be different from antenna to antenna. The min. and max. lengths being considered for this analysis are 10m and 150m respectively. These lengths are a worst-case approximation of the lengths required for an elliptical station geometry 120m x 100m. Two cable types are also discussed, a baseline Kingsignal KSR-200, and an inexpensive RG-58/U cable [2]. The loss formulas for the KSR-200 and RG-58 per meter length are shown in equations 1 & 2 respectively and compared graphically in figure 3 for 150m length. The variation in loss due to temperature, aging and other factors are assumed to be less than 3dB and are not accounted for in this analysis.

$$L_{ksr200} = \ell_m(0.01053\sqrt{F_{mhz}} + 0.0000108F_{mhz}) \quad (1)$$

$$L_{rg58} = \ell_m(0.0014F_{mhz} + 0.05) \quad (2)$$

where ℓ_m is the cable length in meters and F_{mhz} is the frequency in MHz.

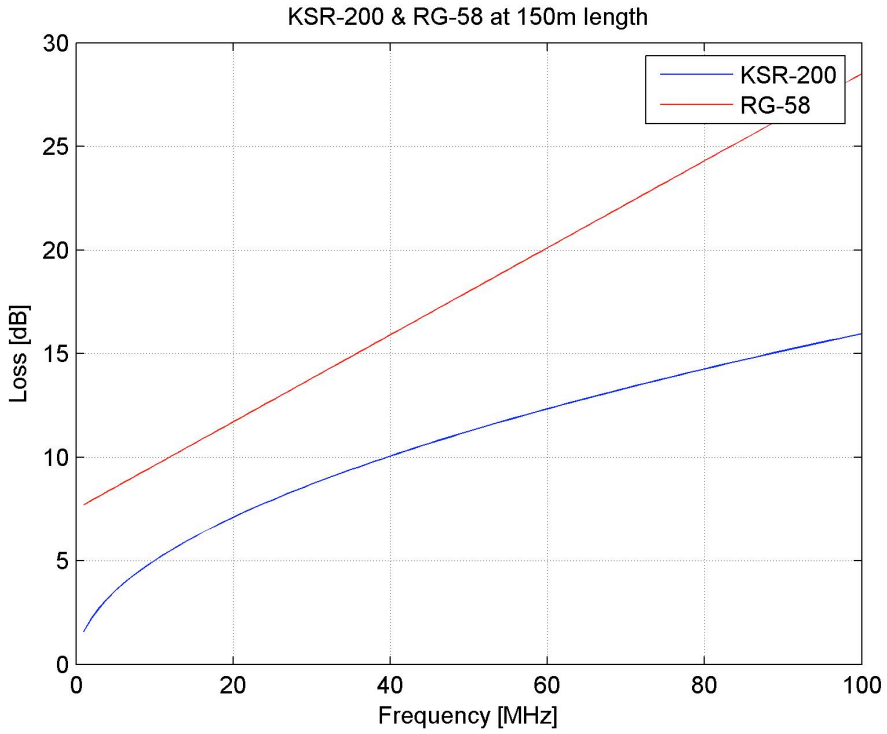

Figure 3: KSR-200 & RG-58 loss over frequency for 150m cable

At 150m, KSR-200 has a loss between 5dB and 15dB (10MHz and 90MHz). RG-58 has a loss of 10dB to 27dB (10MHz to 90MHz) at 150m. At 10m, KSR-200 has a loss of 1dB and RG-58 has a loss of 2dB. These are the losses that are analyzed in tables 4 & 5. The ARX GNI metrics use were determined from the above analysis. The purpose of this GNI analysis is to see what affects the loss variance in the RPD will have on the analog signal path GNI.

RG-58, 150m, 90MHz

	Stage Characteristics			System Characteristics		
	Gain [dB]	**Noise Figure [dB]**	**IIP3 [dBm]**	**Gain [dB]**	**Noise Figure [dB]**	**IIP3 [dBm]**
FEE - RTA	35.0	2.7	-2.3	35.0	2.7	-2.3
RPD - RG-58, 150m, 90MHz	-27.0	27.0	200.0	8.0	3.1	-2.3
SEP	-1.0	1.0	200.0	7.0	3.1	-2.3
ARX	17.4 to 62.4	10.5 to 3.8	+8.2 to -25.9	**24.4 to 69.4**	**6.1 to 3.7**	**-3.9 to -32.9**

RG-58, 150m, 10MHz

	Gain [dB]	**Noise Figure [dB]**	**IIP3 [dBm]**	**Gain [dB]**	**Noise Figure [dB]**	**IIP3 [dBm]**
FEE - RTA	35.0	2.7	-2.3	35.0	2.7	-2.3
RPD - RG-58, 150m, 10MHz	-10.0	10.0	200.0	25.0	2.7	-2.3
SEP	-1.0	1.0	200.0	24.0	2.7	-2.3
ARX	17.4 to 62.4	10.5 to 3.8	+8.2 to -25.9	**41.4 to 86.4**	**2.8 to 2.72**	**-16 to -49.9**

RG-58, 10m

	Gain [dB]	**Noise Figure [dB]**	**IIP3 [dBm]**	**Gain [dB]**	**Noise Figure [dB]**	**IIP3 [dBm]**
FEE - RTA	35.0	2.7	-2.3	35.0	2.7	-2.3
RPD - RG-58, 10m	-2.0	2.0	200.0	33.0	2.7	-2.3
SEP	-1.0	1.0	200.0	32.0	2.7	-2.3
ARX	17.4 to 62.4	10.5 to 3.8	+8.2 to -25.9	**49.4 to 94.4**	**2.7 to 2.7**	**-23.8 to -57.9**

Table 4: Analog Signal Path GNI with RG-58

KSR-200, 150m, 90MHz

	Stage Characteristics			System Characteristics		
	Gain [dB]	**Noise Figure [dB]**	**IIP3 [dBm]**	**Gain [dB]**	**Noise Figure [dB]**	**IIP3 [dBm]**
FEE - RTA	35.0	2.7	-2.3	35.0	2.7	-2.3
RPD - KSR200, 150m, 90MHz	-15.0	15.0	200.0	20.0	2.7	-2.3
SEP	-1.0	1.0	200.0	19.0	2.7	-2.3
ARX	17.4 to 62.4	10.5 to 3.8	+8.2 to -25.9	**36.4 to 81.4**	**3.0 to 2.8**	**-11.4 to -44.9**

RG-58, 150m, 10MHz

	Gain [dB]	**Noise Figure [dB]**	**IIP3 [dBm]**	**Gain [dB]**	**Noise Figure [dB]**	**IIP3 [dBm]**
FEE - RTA	35.0	2.7	-2.3	35.0	2.7	-2.3
RPD - KSR200, 150m, 10MHz	-5.0	5.0	200.0	30.0	2.7	-2.3
SEP	-1.0	1.0	200.0	29.0	2.7	-2.3
ARX	17.4 to 62.4	10.5 to 3.8	+8.2 to -25.9	**46.4 to 91.4**	**2.7 to 2.7**	**-20.9 to -54.9**

RG-58, 10m

	Gain [dB]	**Noise Figure [dB]**	**IIP3 [dBm]**	**Gain [dB]**	**Noise Figure [dB]**	**IIP3 [dBm]**
FEE - RTA	35.0	2.7	-2.3	35.0	2.7	-2.3
RPD - KSR200, 10m	-1.0	1.0	200.0	34.0	2.7	-2.3
SEP	-1.0	1.0	200.0	33.0	2.7	-2.3
ARX	17.4 to 62.4	10.5 to 3.8	+8.2 to -25.9	**50.4 to 95.4**	**2.7 to 2.7**	**-24.8 to -58.9**

Table 5: Analog Signal Path GNI with KSR-200

It was determined above that in max. gain configuration, the IIP3 should be -64dBm or better to achieve decent linearity. This holds true for both cables at all lengths, over all frequencies. In min. gain configuration, the IIP3 should be -19dBm or better to achieve decent linearity. This holds true for both cables at 150m lengths only. The shorter the cable, the less flexibility there is to attenuate strong RFI signals. Both cables will exhibit increased nonlinearities as the cable runs get shorter.

One solution is to use the two 31dB step attenuators to provide some additional attenuation to equalize the gains across cable lengths. For example, the worst case is when the RPD provides only 1dB of loss. Setting SA1 and SA2 to maximum attenuation, the following GNI is produced (Table 6). With a 10m cable (either type) the proper system gain is achieved and the linearity is now much better. The trade-off comes in the number of control bits required. The two 31dB step attenuators require 6 bits each to achieve full attenuation. It is possible to latch certain bits (1dB, 2dB, 4dB) so that less control logic is required, but it is desirable to latch these at 0dB instead of

their respective attenuation. With 32 channels per ARX module and 6 bits per channel, 192 bits of control are needed. Being able to group the control of channels will reduce the number of logic bits. With channel grouping, a set of antennas would change gain instead of individual control.

Min. Gain (G = +4dB)	**Stage Characteristic**			**ARX Characteristic**		
Component	**Gain [dB]**	**NF [dB]**	**IIP3 [dBm]**	**Gain [dB]**	**NF [dB]**	**IIP3 [dBm]**
Coaxial Relay	-1.0	1.0	200.0	-1.0	1.0	200.0
A1 - Gali74	25.1	2.7	12.9	24.1	3.7	13.9
SW1 - S0192	0.2	0.2	53.0	23.9	3.7	13.8
SW2 - S0192	0.2	0.2	53.0	23.7	3.7	13.8
BPF1	-1.5	1.5	200.0	22.2	3.7	13.8
SW3 - S0192	0.2	0.2	53.0	22.0	3.7	13.7
SW4 - S0192	0.2	0.2	53.0	21.8	3.7	13.7
SA1 - DAT31	-19.3	19.3	52.0	-10.5	11.3	13.6
A2 - Gali74	25.1	2.7	12.9	14.6	13.7	13.2
BPF2	-1.5	1.5	200.0	13.1	13.7	13.2
SA2 - DAT31	-32.3	32.3	52.0	-19.2	20.3	13.1
A3 - Gali74	25.1	2.7	12.9	5.9	22.5	13.1
BPF3	-1.5	1.5	200.0	**4.4**	**22.5**	**13.1**

Min. Gain Configuration	**Stage Characteristic**			**System Characteristic**		
Stage	**Gain [dB]**	**NF [dB]**	**IIP3 [dBm]**	**Gain [dB]**	**NF [dB]**	**IIP3 [dBm]**
FEE - RTA	35.0	2.7	-2.3	35.0	2.7	-2.3
RPD - KSR-200, 10m	-1.0	1.0	200.0	20.0	2.7	-2.3
SEP	-1.0	1.0	200.0	33.0	2.7	-2.3
ARX	4.4	22.5	13.1	**37.4**	**2.9**	**-20.0**

Table 6: Analog Signal Path GNI with short cable attenuation

Optimizing the ARX signaling for 150m cable has the advantage of reducing the GNI frequency dependence, but doesn't perform well with short cable lengths. Other solutions to equalizing cable loss could be making all cables the same length or inserting additional attenuation somewhere else in the signal path. A more complex architecture may switch amplifiers out of the signal path to achieve better system GNI. The block-diagram and GNI analysis in this document show that the requirements from LWA Memo 121 are achievable with a simple, low-cost analog receiver architecture.

References:

[1] S. Ellingson, "LWA Analog Signal Path Planning, Version 2," LWA Memo 121, Feb 3,2008.

[2] Aaron Kerkhoff, John Copeland, and Brian Hicks, "LWA RF and Power Distribution Design - v0.1," LWA EM RPD0001, March 13, 2008.

[3] Chaitali R. Parashare and Richard Bradley, "120-205 MHz Receiver for PAPER: Precision Array to Probe the Epoch of Reionization," NRAO NTC-DSL Laboratory Report, December, 2006.

LWA Engineering Memo

ARX Strawman Design

Task: ARX0004-A
Joe Craig
May 1, 2008

1. Detailed Design

ARX0003 [1] provided a first-look block diagram of the ARX signal path. Figure 1 is an in-depth block diagram which includes other ARX components being considered such as a bias-T for powering the Front-End Electronics (FEE), coupled test connections, monitor and control interface, and a diplexer filter section.

The bias-T can be designed with lumped element components (capacitors & inductors). Designing the bias-T into the ARX as opposed to a connectorized version in the Shelter Entry Panel (SEP) reduces the station cost by about 2% since lumped elements are an insignificant cost compared to connectorized bias-Ts (~$40 each from RPD0002 [2]). The risk in using a lumped element bias-T in the ARX comes in impedance matching. The lumped element bias-T may significantly increase VSWR and require an additional matching network. Surface-Mount bias-Ts exist (fully matched) but are comparable in price to a connectorized version.

A cable loss equalizing attenuator is included to provide a method for equalizing the distributed losses from unequal cable lengths. It is assumed that all 512 ARX channels will share common gain and configuration control which results in a large gain (and effectively linearity) variation from antenna to antenna due to different lengths of cable (see ARX0003 for more information). A digital step attenuator with 15dB of attenuation in 2dB steps should be sufficient. The cable loss equalizing attenuator is the only way to control channel gains independently. An alternative method of equalizing channel gains is to quantize cable runs to a few certain lengths and have a few fixed attenuators in the ARX as compensation. Each ARX channel would then correspond to an RPD cable length.

Two directional couplers are provided to view the signals coming in and leaving the ARX for diagnostic and development purposes. Feedpoints are also included for injecting signals into the system. The ARX circuit board should provide flexibility to 'load' or "unload' the test connectors and terminate the coupled and isolated ports of the directional couplers. The production ARX will most likely have terminated isolated ports and only a few loaded test connectors on the coupled port.

The reconfigurable filter section has been designed for a single pair of SP3T configuration switches as opposed to the cascaded switch architecture in ARX0003. RF switches are notorious for poor return loss and parasitic effects and therefore should not

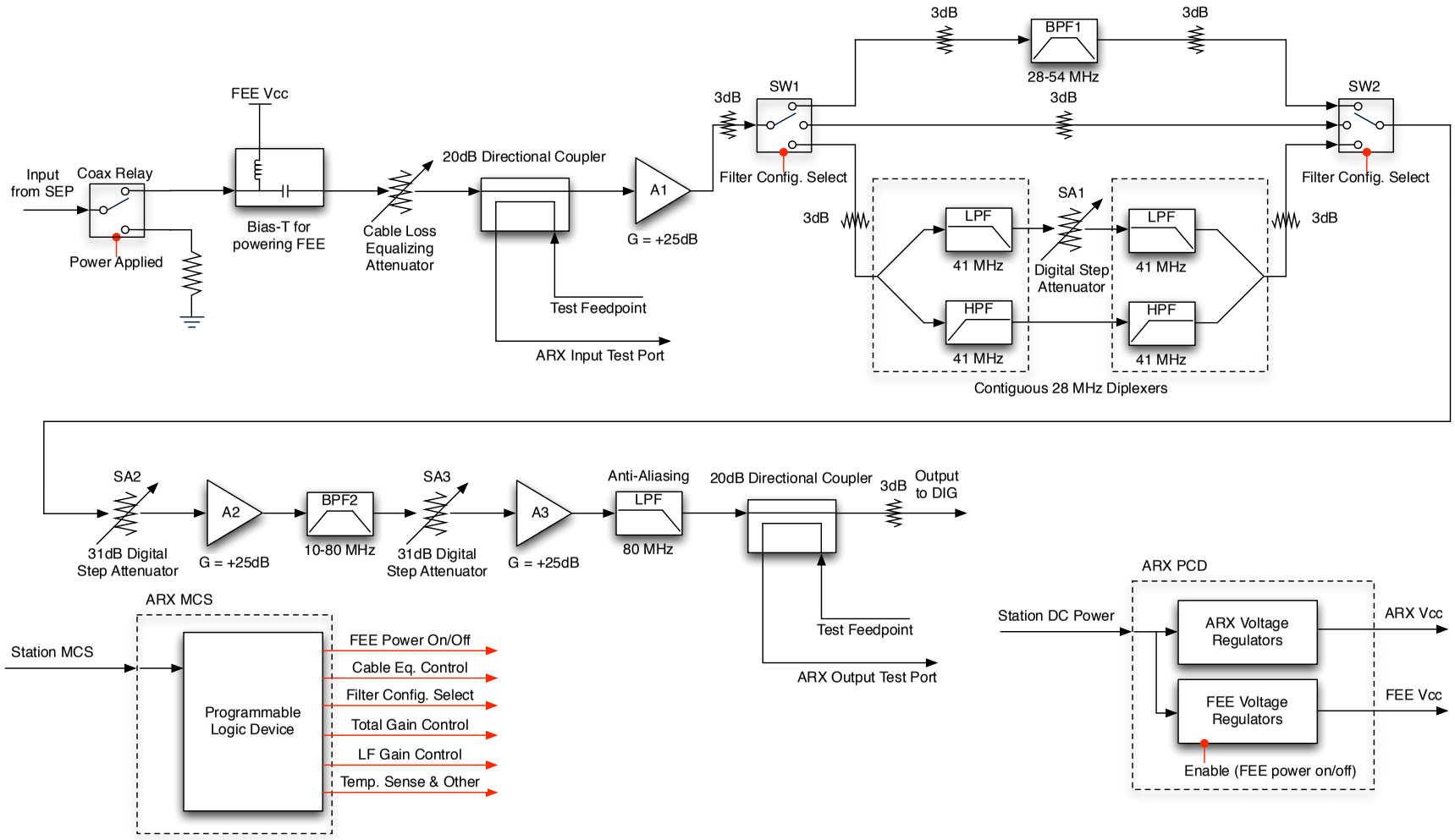

Figure 1: ARX Block Diagram

be cascaded. An additional level of protection against standing-waves (VSWR) is provided by including 3dB attenuators wherever the switch mismatch occurs. After testing and circuit optimization, it may be decided that little to no attenuation (for impedance matching) is required between these stages.

The back-to-back diplexer filter section discussed in section 1.3 of ARX0004 [3] provides a method of gain controlling frequency bands independently. The filters are singly-terminated and contiguous (share the same 3dB point) to provide a good match at all frequencies. A cutoff of 41 MHz is desired to attenuate the amplitude varying low-frequency RFI, independent of the gain of the entire bandwidth. A 31dB step attenuator in 1dB steps should be sufficient for the level of low-frequency gain control required. The diplexer is duplicated and mirrored to provide lossless signal combining. A future engineering memo will discuss the design details of the diplexer and other filters used in the ARX design.

The ARX Monitor and Control block is provided to illustrate the control signals required to configure the ARX channels. This digital block may be physically separated from the ARX circuit board to isolate the digital circuit signals (clocks, etc.) from the analog receive path. There are no timing critical signals or advanced signal processing requirements for the ARX digital control (basically just static logic), therefore, the digital control may be implemented in a cost-effective microcontroller, PIC, or other PLD (FPGA is probably overkill). In addition to controlling the ARX configurations and gains, the logic device will also need to control the powering of the FEEs and reading temperature sensor information (if required).

The ARX power is assumed to be derived from a single DC supply voltage. Each ARX channel has an independent voltage regulator for the FEE to enable and disable power out to each antenna. The regulated voltages to power the amplifiers and other components in each ARX channel may be consolidated to a few regulators on the circuit board or have separate regulators for each channel like the FEE power.

Depending on the amplifiers used, the voltages required on the ARX circuit board could be between +7 VDC and +15 VDC for the analog gain stage power. Assuming the gain stages are Gali-74 amplifiers, each channel will draw approximately 250mA (80mA * 3 stages) from the analog gain stage regulators. The digital components (step attenuators, PLD, etc.) will require +5 VDC and possible +3.3 VDC and should total no more than 500mA per ARX module. The switches (assuming GaAs technology) draw minimal current (on the order of a few uAmps) and can operate on the +5 VDC digital supply. Assuming the four variable attenuators are DAT-31 digital step attenuators, they will draw 100uA each, resulting in 0.5mA per channel. The FEE voltage is +15 VDC feeding the bias-Ts and draws approximately 230mA [4]. Separate voltage regulators should be provided for the analog gain stages, digital components, and FEE bias-T power to reduce the amount of cross-coupling noise between supply voltages. Since the highest voltage required is +15 VDC, it is recommended that the station DC voltage into the ARX module be at least 1V higher (+16 VDC) although a standard module voltage of +18 VDC may be chosen. An alternative to including the FEE regulators on

the ARX circuit board would be to include them in a separate “FEE PCD” module, controlled by the ARX. A summary of ARX current demands are listed below for ARX modules with a number of different channels.

Power Section	4 channels	16 channels	32 channels
FEE Bias-T Power (Assuming FEE G250R)	920mA @ +15 VDC	3.68A @ +15 VDC	7.36A @ +15 VDC
Analog Gain Stage Power (Assuming 3 Gali-74 amps)	1A @ +9 VDC	4A @ +9 VDC	8A @ +9 VDC
Digital Circuitry Power	500mA @ +5 VDC	500mA @ +5 VDC	500mA @ +5 VDC
Total:	**2.42A**	**8.18A**	**15.86A**

Table 1: Total current consumption for an ARX module of 4, 16, and 32 channels

The amount of digital logic required to control each ARX channel is substantial. Controlling the gain in 4dB steps should be satisfactory, therefore, if DAT-31 step attenuators are used (31dB of attenuation, 5 bit parallel control, 1dB LSB), two bits may be tied high (or low) to reduce the number of digital control lines required. The LF Gain control (diplexer 3-41 MHz band) may need control in 1dB steps, therefore will require the full 5 bits of control logic. The cable loss equalizing attenuator should have sufficient control with 4dB steps and would only require 3 bits of control logic (same as the two gain control attenuators), however, needs to be independently controlled. Table 2 summarizes the required logic assuming each channel’s cable loss equalizing attenuator operates independently and the gain control is uniformly controlled.

The cable loss equalization control logic has the most potential for I/O reduction. An alternative to independent channel control, is to group channel equalization control together. Each grouping reduces the bit count by 3 bits. In the 32 channel ARX module case, if groups of 4 channels per cable loss equalization control were implemented, the number of I/O required drops from 142+ bits to 70+ bits. Although, it may be more beneficial to get rid of the variable attenuators all together and implement groupings of fixed attenuators (requiring 0 bits of control). Channels 1-4 could have 0dB attenuators (corresponding to cable lengths of 150m); channels 5-8 could have 3dB attenuators (corresponding to cable lengths of 120m); channels 9-12 could have 6dB attenuators (corresponding to cable lengths of 90m); channels 13-16 could have 9dB attenuators (corresponding to cable lengths of 60m); channels 17-20 could have 12dB attenuators (corresponding to cable lengths of 30m); and the rest of the channels could have 15dB attenuators (corresponding to cable lengths of less than 30m). Obviously an appropriate distribution of attenuator values from station cable lengths should be determined.

Logic Section	4 channels	16 channels	32 channels
FEE Power On/Off (1 bit/channel)	4 bits	16 bits	32 bits
Cable EQ Control (3 bits/channel)	12 bits	48 bits	96 bits
Filter Config. Select (3 bits total)	3 bits	3 bits	3 bits
Total Gain Control (6 bits total)	6 bits	6 bits	6 bits
LF Gain Control (5 bits total)	5 bits	5 bits	5 bits
Temp Sense/Other	unknown	unknown	unknown
Total Bits Required:	**30+ bits**	**78+ bits**	**142+ bits**

Table 2: Control bits required for and ARX module of 4, 16, and 32 channels

Some other detailed design considerations that should be mentioned as part of the Analog Signal Processor (ASP) are the possible need for temperature monitoring, fan speed control, and current sensing circuitry. The large amount of power distribution that may be located in the ARX and the amount of gain per channel indicates a possible need for temperature monitoring and control. The analog filters will be susceptible to temperature fluctuations ultimately decreasing relative gain and phase stability. A simple PID controller may be implemented with the ARX Monitor/Control logic.

2. **Candidate Components**

The critical components for selection in the ARX signal path are the amplifiers, step attenuators, switches, filters, voltage regulators, bias-Ts, couplers, coaxial relays, and connectors. Other components relating to the logic circuit, monitor and control, and power supplies also need to be considered. Tables 3 and 4 show amplifier and step attenuator options available with their critical parameters (an archived folder of datasheets is included as an appendix). Other components will be addressed in future Engineering Memos.

	Hittite	Mimix	MCL	MCL	MCL	Aeroflex	M/A Com	M/A Com	M/A Com	WJ	WJ
	HMC580ST89	CGB7289-SC	Hela-10D	Gali-74+	MERA-7433	MMA710	A59/SMA59	A101/SMA101	A79/SMA79	EC1078B	ECG004B
Comment			high current, support circuitry		dual-channel						low current
Frequency (MHz)	DC-1000	DC-2500	8-300	DC-1000	DC-1000	DC-4000	2-700	3-120	2-350	DC-3500	DC-6000
Gain [dB]	22	21	11	25.1	25	13	12	18	14	21	17
Noise Figure [dBm]	2.8	3.8	9.4	2.7	2.5	4.8	5.4	2.7	5	3.2	3.3
IP1dB [dBm]	0	2.3	19	-5.9	-6	9	10	4.7	8.5	-1	3.5
IIP3 [dBm]	15	19	37	13	11.5	26	28	21	24	16	10
Supply Voltage (VDC)	5-8	9-12	12	7-15	7-15	8-15	15	12	15	7-12	5-12
Supply Current (mA)	88	120	525	80	160	95	88	105	88	96	35
Package	SOT	SOT	SOT w/GND slug	SOT	LLC w/GND slug	SOT	TO & SOT	TO & SOT	TO & SOT	SOT	SOT
Price, Q > 1000	???	???	$16	$2.35	$4.70	???	???	???	???	???	???

Table 3: Candidate Amplifiers

	Hittite	Hittite	Hittite	Hittite	MCL	MCL	M/A Com	SkyWorks	SkyWorks
	HMC470LP3	HMC307QS16G	HMC541LP3	HMC629LP4	DAT-31-PP	TOAT-51020	AT-106-PIN	AA117-85	SKY12332-310LF
Comment		negative supply & logic		serial or parallel control		Pin Diode	Dual Supplies	Dual Supplies	low RF noise floor
Frequency (MHz)	DC-3000	DC-4000	DC-5000	DC-6000	DC-2400	10-1000	DC-2000	LF-2000	LF-1000
Number of Bits	5	5	1	4	5	3	6	5	6
Maximum Attenuation [dB]	31	31	10	45	31	35	50	31	31.5
LSB step [dB]	1	1	10	3	1	5	1	1	0.5
Insertion Loss [dB]	1.2	1.8	0.5	2	1.3	4	2.5	1.4	1.5
IIP3 [dBm]	45	44	50	???	52	???	34	46	36
Supply Voltage (VDC)	5	-5	5	5	3	5.5	5 & -5	5 & -3	5
Package	LLC w/GND slug	SOP w/GND slug	LLC w/GND slug	LLC w/GND slug	LLC w/GND slug	TO	SOP w/GND slug	SOP	LLC w/GND slug
Price, Q > 1000	???	???	???	???	$3.50	$64	???	???	???

Table 4: Candidate Digital Step Attenuators

3. **Detailed GNI**

ARX0003 provided a first-look at the Analog Signal Path GNI. Based on the block diagram given in Figure 1, the GNI analysis for the ARX in maximum gain configuration can be generated (Table 5). The table shows an estimated ARX GNI in full-bandwidth, maximum gain configuration, based on three Gali-74 amplifiers and two TOAT-51020 diode step attenuators. The bottom portion of the table is the ASP GNI using the ARX metrics (for 150m of RG-58 cabling and an G250R active balun).

Max. Gain (G = +48dB)	**Stage Characteristic**			**ARX Characteristic**		
Component	**Gain [dB]**	**NF [dB]**	**IIP3 [dBm]**	**Gain [dB]**	**NF [dB]**	**IIP3 [dBm]**
Coax Relay	-1.0	1.0	200.0	-1.0	1.0	200.0
biasT	-0.5	0.5	200.0	-1.5	1.5	197.5
attn1	-3.0	3.0	200.0	-4.5	4.5	196.0
coupler1	-0.3	0.3	200.0	-4.8	4.8	195.4
A1-gali74	25.0	2.7	13.0	20.2	7.5	17.8
attn2	-3.0	3.0	200.0	17.2	7.5	17.8
filters	-6.0	6.0	40.0	11.2	7.6	16.6
stepAttn1	-4.0	4.0	200.0	7.2	7.6	16.6
A2-gali74	25.0	2.7	13.0	32.2	7.8	5.5
BPF	-1.0	1.0	200.0	31.2	7.8	5.5
stepAttn2	-4.0	4.0	200.0	27.2	7.8	4.9
A3-gali74	25.0	2.7	13.0	52.2	7.8	-14.3
LPF	-1.0	1.0	200.0	51.2	7.8	-14.3
coupler2	-0.3	0.3	200	50.9	7.8	-14.3
attn3	-3	3	200	**47.9**	**7.8**	**-14.3**

Max. Gain Configuration	**Stage Characteristic**			**System Characteristic**		
Stage	**Gain [dB]**	**NF [dB]**	**IIP3 [dBm]**	**Gain [dB]**	**NF [dB]**	**IIP3 [dBm]**
FEE - RTA	35.0	2.7	-2.3	35.0	2.7	-2.3
RPD - RG58	-15.0	15.0	200.0	20.0	2.7	-2.3
ARX	**47.9**	**7.8**	**-14.3**	**67.9**	**2.8**	**-34.3**

Table 5: GNI with lossiest signal path, 3 Gali-74 amplifiers

The ARX gain in the above analysis does not meet the requirements from ARX0003. An additional amplifier (A101/SMA101) and 3dB attenuator will be added before the anti-aliasing filter to determine the effects on the analog signal path GNI if a fourth amplifier is needed (Table 6). With a fourth amplifier, the ARX now meets the gain requirement, and the linearity meets specification. Also, the minimum gain configuration is shown in Table 7 to illustrate the poor noise figure obtained when a lossy signal path is required.

Max. Gain (G = +63dB)	**Stage Characteristic**			**ARX Characteristic**		
Component	**Gain [dB]**	**NF [dB]**	**IIP3 [dBm]**	**Gain [dB]**	**NF [dB]**	**IIP3 [dBm]**
Coax Relay	-1.0	1.0	200.0	-1.0	1.0	200.0
biasT	-0.5	0.5	200.0	-1.5	1.5	197.5
attn1	-3.0	3.0	200.0	-4.5	4.5	196.0
coupler1	-0.3	0.3	200.0	-4.8	4.8	195.4
A1-gali74	25.0	2.7	13.0	20.2	7.5	17.8
attn2	-3.0	3.0	200.0	17.2	7.5	17.8
filters	-6.0	6.0	40.0	11.2	7.6	16.6
stepAttn1	-4.0	4.0	200.0	7.2	7.6	16.6
A2-gali74	25.0	2.7	13.0	32.2	7.8	5.5
BPF	-1.0	1.0	200.0	31.2	7.8	5.5
stepAttn2	-4.0	4.0	200.0	27.2	7.8	4.9
A3-gali74	25.0	2.7	13.0	52.2	7.8	-14.3
attn3	-3.0	3.0	200.0	49.2	7.8	-14.3
A4-A01	18	2.7	21	67.2	7.8	-28.4
LPF	-1	1	200	66.2	7.8	-28.4
coupler2	-0.3	0.3	200	65.9	7.8	-28.4
attn3	-3	3	200	**62.9**	**7.8**	**-28.4**

Max. Gain Configuration	**Stage Characteristic**			**System Characteristic**		
Stage	**Gain [dB]**	**NF [dB]**	**IIP3 [dBm]**	**Gain [dB]**	**NF [dB]**	**IIP3 [dBm]**
FEE - RTA	35.0	2.7	-2.3	35.0	2.7	-2.3
RPD - RG58	-15.0	15.0	200.0	20.0	2.7	-2.3
ARX	**62.9**	**7.8**	**-28.4**	**78.9**	**2.8**	**-45.5**

Table 6: GNI with lossiest signal path, 3 Gali-74 amplifiers and 1 A101 amplifier

Min. Gain (G = +18dB)	**Stage Characteristic**			**ARX Characteristic**		
Component	**Gain [dB]**	**NF [dB]**	**IIP3 [dBm]**	**Gain [dB]**	**NF [dB]**	**IIP3 [dBm]**
Coax Relay	-1.0	1.0	200.0	-1.0	1.0	200.0
biasT	-0.5	0.5	200.0	-1.5	1.5	197.5
attn1	-3.0	3.0	200.0	-4.5	4.5	196.0
coupler1	-0.3	0.3	200.0	-4.8	4.8	195.4
A1-gali74	25.0	2.7	13.0	20.2	7.5	17.8
attn2	-3.0	3.0	200.0	17.2	7.5	17.8
filters	-6.0	6.0	40.0	11.2	7.6	16.6
stepAttn1	-14.0	14.0	200.0	-2.8	8.8	16.6
A2-gali74	25.0	2.7	13.0	22.2	9.6	13.2
BPF	-1.0	1.0	200.0	21.2	9.6	13.2
stepAttn2	-39.0	39.0	200.0	-17.8	18.4	13.2
A3-gali74	25.0	2.7	13.0	7.2	20.8	13.1
attn3	-3.0	3.0	200.0	4.2	20.9	13.1
A4-A01	18	2.7	21	22.2	20.9	11.6
LPF	-1	1	200	21.2	20.9	11.6
coupler2	-0.3	0.3	200	20.9	20.9	11.6
attn3	-3	3	200	**17.9**	**20.9**	**11.6**

Min. Gain Configuration	**Stage Characteristic**			**System Characteristic**		
Stage	**Gain [dB]**	**NF [dB]**	**IIP3 [dBm]**	**Gain [dB]**	**NF [dB]**	**IIP3 [dBm]**
FEE - RTA	35.0	2.7	-2.3	35.0	2.7	-2.3
RPD - RG58	-15.0	15.0	200.0	20.0	2.7	-2.3
ARX	**17.9**	**20.9**	**11.6**	**37.9**	**4.9**	**-9.4**

Table 7: GNI with lossiest signal path (minimum gain configuration), 3 Gali-74 amplifiers and 1 A101 amplifier

From this analysis, it is determined that minimizing the losses in the ARX signal path is very important to maintain decent analog signal path performance across all gain configurations. If the loss due to the matching attenuators is minimized and low insertion-loss components are chosen, it is very possible that only three Gali-74 amplifiers (or other amplifiers equivalent to 75dB of gain) would be required. The only way this can be determined is through laboratory testing of prototype analog receivers. In the event that a fourth amplifier is required, it has been shown that although linearity will suffer slightly, IIP3 is still within specification. The system temperature (noise figure) suffers greatly however, especially when using the minimum gain configuration. This is yet another argument for having a low-shelf filter configuration; the system temperature will be dependent on frequency, i.e. the low frequency band will have the poor noise figure (which is tolerable) while the upper frequency band can maintain a low noise figure.

5. **ARX Requirements**

Using the information from LWA Memo 121 [5], ARX0003, and ARX0004, an initial set of ARX requirements can be noted:

ARX Parameter	**Max. Gain Configuration**	**Min. Gain Configuration**
Gain	$\geq$ 62dB	$\leq$ 17dB
Linearity (IP1dB)	$\geq$ -62dBm	$\geq$ -17dBm
Linearity (IIP3)	$\geq$ -47dBm	$\geq$ -2dBm
Noise Figure	$\leq$ 7dB	TBD
3dB Bandwidth: Full BW Configuration	20 MHz to 80 MHz (3 MHz to 88 MHz desired)	20 MHz to 80 MHz (3 MHz to 88 MHz desired)
Passband Ripple	TBD	TBD
Rejection at 1 MHz	TBD	TBD
Rejection at 90 MHz	TBD	TBD
Gain Stability	TBD	TBD
Phase Stability	TBD	TBD
Input Return Loss	TBD	TBD
Output Return Loss	TBD	TBD

Table 8: ARX Requirements

These requirements are intended to identify the important ARX parameters to be considered. The requirements are shown for full bandwidth configuration and will change with each filter configuration. Future ARX requirements should be documented separately by ARX mode (filter configuration).

Minimum Gain metric is derived from the gain required to digitize a maximum signal level of -54dBm (seen at FEE inputs). Maximum Gain metric is the gain required to allow 45dB of gain control from minimum gain configuration. Linearity numbers were derived in LWA Memo 121 based on maximum signal level of -54dBm and scaled dB for dB with gain. The noise figure metric is that which maintains a system temperature of the entire receiver, close to that of the front-end electronics. The 3dB bandwidth metrics (for full bandwidth configuration) are noted from the requirements in the LWA Scientific

Requirements document [6]. The TBD metrics are intended as placeholders and must be discussed and agreed upon in future ARX requirements documentation.

References:

[1] Joe Craig, “Analog Signal Path GNI and ARX Block Diagram v.1,” LWA EM ARX0003, April 11, 2008

[2] Aaron Kerkhoff, John Copeland, and Brian Hicks, “LWA RF and Power Distribution Design - v0.2,” LWA EM RPD0002, April 21, 2008.

[3] Joe Craig, “ARX Reconfigurable Filter Options,” LWA EM ARX0004, May 1, 2008

[4] Brian Hicks and Nagini Paravastu, “The Rapid Test Array Balun (G250R),” LWA Memo 120, Dec. 12, 2007

[5] Steve Ellingson, “LWA Analog Signal Path Planning, Version 2,” LWA Memo 121, Feb. 3, 2008.

[6] Tracy E. Clarke, “Scientific Requirements for the Long Wavelength Array,” LWA Memo 117, Nov. 19, 2007

LWA Engineering Memo

RF Switch Options

Task: ARX0005
Joe Craig
May 9, 2008

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In order to select a configuration of the ARX filters, an RF switch must be used. Similarly, in order to protect the ARX receiver when not powered, an RF relay switch must be used. This document details the different options for RF switches, considering electro-mechanical switches for input protection, and two methods of switching for filter selection (PIN diode circuit and drop-in components).

1. Coaxial Relays

The coaxial relay is required to protect the receiver inputs when the station is not in use. Table 1 details candidate coaxial relay switches available. A major design consideration with this component is cost. Electro-mechanical RF relays can easy cost $100 each. SPDT relays are being considered only. Datasheets are provided as an appendix to ARX0005.

	Teledyne 431T	Tohtsu CX-120P	Tyco HF3	Teledyne RF311
comment:	range of coil voltages available	used in ETA receivers	latching/non-latch, single/dual coil available	range of coil voltages available
Coil Voltage	12V	10V - 14V	9V - 26V	12V
Frequency (MHz)	DC-1000	DC-1000	DC-3000	DC-8000
Isolation	55dB	60dB	85dB	45dB
Coil Current	10mA @ 12V	61mA @ 12V	12mA @ 12V	16mA
VSWR/Return Loss	35dB	32dB	35dB	35dB
Insertion Loss [dB]	0.1dB	0.1dB	0.1dB	0.1dB
Package	TO-5	large package	surface mount	TO-5
Price, Q > 1000	$36	$28	$2.67	$35

Table 1: Candidate Coaxial Relays

The Tyco HF3 looks very promising and no parameter has been identified that would prevent it from being evaluated in early ARX prototypes. The Tohtsu CX-120P is a fall-back solution, but should be prevented in the final ARX design due to it's large package size.

2. **PIN Diode Switch**

Positive Intrinsic Negative (PIN) diodes are commonly used for RF circuits because of their linear IV curve when forward biased. They can be used as variable resistors (for variable attenuator applications) or on/off switches with low forward-biased resistances and high isolation. Traditional, non-linear diodes can not be used due to their large forward-biased resistance. At lower frequencies, the PIN diode acts as a non-linear diode. The linear frequency range depends on the manufacturing process, MELF or HiPAX PIN diodes are most linear at the lower frequency range of LWA. At higher frequencies, the PIN diode acts as a variable resistor. Figure 1 shows an ideal linear response for a PIN diode: higher bias current, lower resistance.

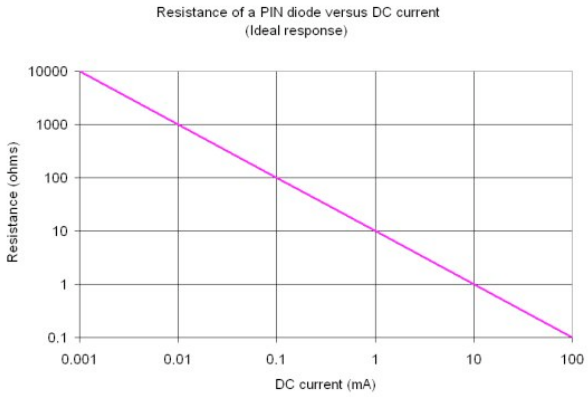

Figure 1: PIN Diode forward-biased resistance curve

RF switch circuits suffer from poor isolation. To obtain decent isolation, the switches are usually cascaded. A series-shunt topology is the preferred topology for good insertion loss, VSWR, and isolation performance. This, of course, comes at the expensive of high DC power consumption. A dual supply is also required to reverse-bias the circuit. Figure 2 is a series-shunt PIN diode switch circuit that provides 40dB of isolation. The circuit is easily modified to provide the SP3T function for the ARX filter configuration selection.

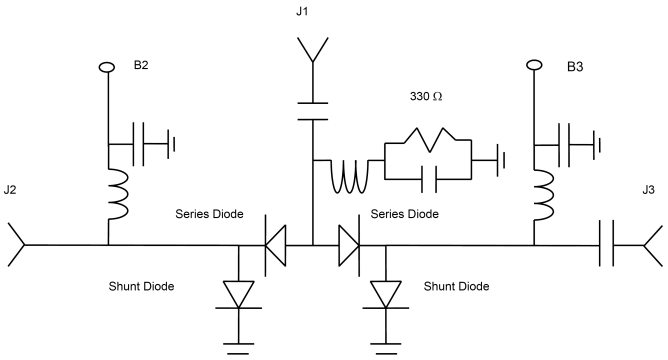

Figure 2: Series-shunt PIN diode switch

2. **Drop-In MMIC Switch**

Drop-In SP3T RF switches should be considered as an alternative to the PIN diode switch circuit. These MMIC switches have the advantage of small size and simplified circuit architecture. There is great difficulty sourcing SP3T RF switches in the LWA frequency range. The few components that have turned up are listed in Table 2. Datasheets are provided in the appendix of ARX0005. It is useful to note that although M/A Com lists a number of candidate components, many of them are not in production or readily available.

	M/A Com	**M/A Com**	**M/A Com**	**Hittite**	**Analog Devices**
	8330	**SS0028**	**SW65-0214**	**HMC245QS16**	**ADG936**
comment:			Integrated ASIC driver	Integrated Driver and 2:1 decoder	Single supply, CMOS drive
Technology	GaAs PHEMT MMIC	GaAs PHEMT MMIC	GaAs MMIC	GaAs MMIC	CMOS
Frequency (MHz)	DC - 3.0 GHz	DC - 3.0 GHz	DC - 3.0 GHz	DC - 3.5 GHz	DC - 2 GHz
Function	SP3T	SP3T	SP3T (absorbtive)	SP3T (absorbtive)	SPDT (absorbtive)
Isolation	24 dB	24 dB	70 dB	45 dB	60 dB
Control Voltage	2.5V	2.5V	3.3V	3.3V	3.3V
Control Current	1 uA	1 uA	none	none	1uA
VSWR/Return Loss	25 dB	25 dB	18 dB	20 dB	25 dB
Insertion Loss [dB]	0.3 dB	0.3 dB	0.75 dB	0.5 dB	0.4 dB
IIP3 [dBm]	50 dBm	50 dBm	35 dBm	51 dBm	33 dBm
Supply Voltage	none	none	+5V & -5V	+5VDC	none
Package	LLC	LLC	SOP	SOP	TSOP
Price, Q > 1000	unavailable	$0.30	unavailable	$3.25	$1.50

Table 2: Candidate drop-in MMIC Switches

The Hittite switch provides internally terminated resistors for non-reflective switch operation. It is easily biased with a +5VDC supply and no logic drivers are required. Logic levels can be 3.3VDC or 5VDC. There is some concern with the return loss when the inputs are in the off state (see return loss plot in the datasheet), therefore, this part should be evaluated before proceeding with selection in the ARX design. However, considering the architecture of the reconfigurable filter, return loss/VSWR performance might not be a concern when the RF1-3 ports are in the “off” state.

Many candidate components are available in SPDT operation, but in order to prevent cascading RF switches, SPDT switches are not considered, except for the Analog Devices switch which has specific application to filter selection (see datasheet).

LWA Engineering Memo

Reconfigurable Filters

Task: ARX0006
Joe Craig
May 21, 2008

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The LWA's analog receivers should provide an extra level of selectivity over the full-bandwidth by utilizing a reconfigurable filter bank. Gain control is used to 'fit' the received signal in the dynamic range of the digitizer, and in the event that strong RFI sources exist, it may be preferred to switch filter configurations from full-bandwidth to a reduced bandwidth so observations at optimal gains can be achieved. This document provides a design for the filter configurations available in the analog receiver as well as a guide to modify these filters for different bandwidths.

The process of designing the filters begins with realizing that LC lumped-elements ladder networks provide the best passive filtering with lowest insertion loss. Prototype lowpass shunt and series ladder networks (cutoff of 1 Hz, load impedance 1 Ohm) are used to find a normalized component value, from a table which has been scaled for both butterworth filter coefficients and termination impedance. The prototype lowpass can be transformed into highpass, bandpass, and bandstop (notch) filters by replacing circuit elements and scaling values. The component values in the schematics provided are standard values, commercial available, and have been tuned and optimized for best return loss performance. Insertion loss and return loss plots are shown for perfect inductors and capacitors with 1% value tolerance. The tolerance was varied over 50 trials to simulate possible S21 (red) and S11 (blue) parameters. A more accurate simulation requires physical component models, so it should be noted, these frequency responses are best-case approximations of actual receiver performance. A design guide for future filter modifications is given in the appendix. The microwave circuit simulator, RFSim99 was used to simulate the filters.

1. 10MHz - 80MHz Full-Bandwidth Filter

A bandpass filter is commonly designed by cascading lowpass and highpass filters and also by combining resonant elements. The resonant structure is usually

reserved for passbands of less than half the highest frequency. For the full bandwidth filter, a 70MHz bandwidth is well above the 40MHz half frequency. However, for completeness, a 10-80MHz bandpass filter is shown below for both structures. Since poles at the low frequency cause faster roll-off than in the high frequency, the circuit elements in a cascaded HPF-LPF network can be minimized by using a lower-order filter for the HPF section, while a higher order is required for the LPF.

Figure 1 shows the circuit elements for a 5th-Order HPF cascaded with a 9th-Order LPF using standard value components. This filter provides better than 60dB attenuation at 1MHz and about 30dB attenuation at 120MHz. Return loss is better than 30dB over most the passband (Figure 2).

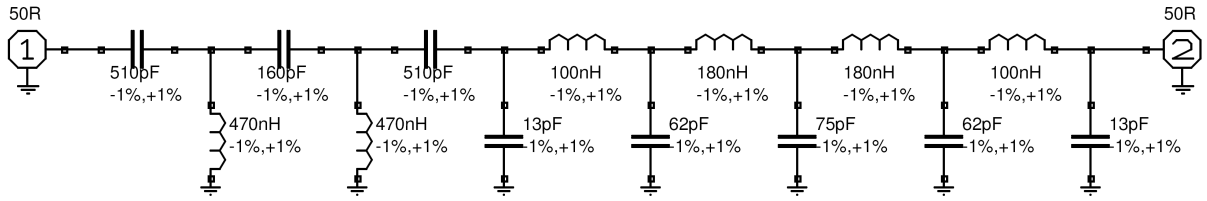


Figure 1: 10MHz - 80MHz, 5th-Order HPF and 9th-Order LPF Circuit

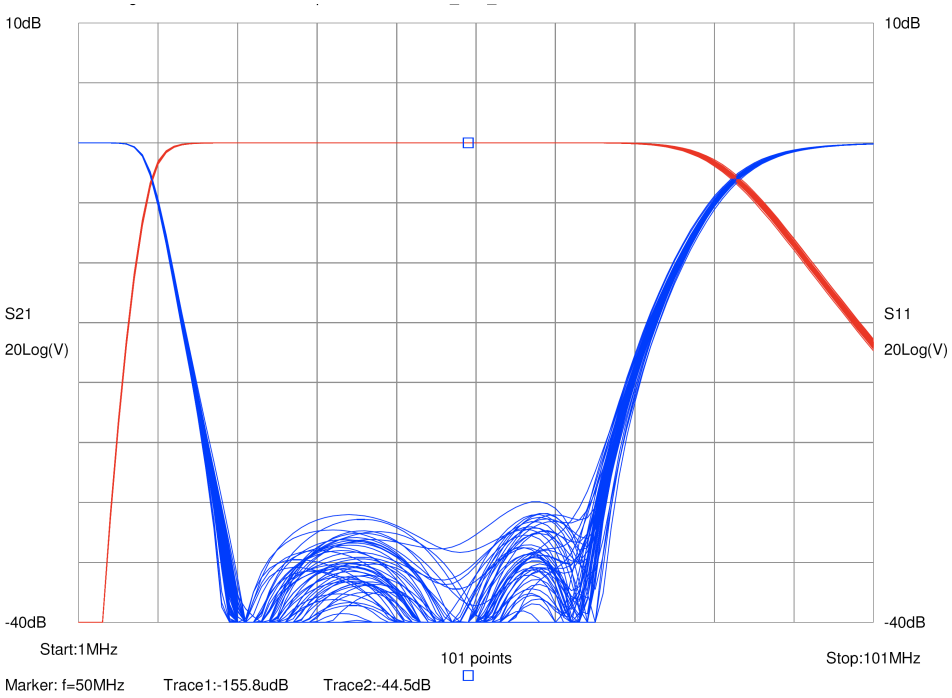


Figure 2: 10MHz - 80MHz, 5th-Order HPF and 9th-Order LPF S21 & S11

Figure 3 shows the circuit elements for a 7th-Order BPF (45MHz center frequency, 70MHz bandwidth) using standard value components. This filter provides 60dB attenuation at 10MHz and about 23dB attenuation at 120MHz. Return loss is better than 20dB over most the passband (Figure 4). For a wideband filter, because of the large variation in roll-off, resonant BPF structures should not be used. The attenuation is too large on the low side of the band and not enough on the high side of the band.

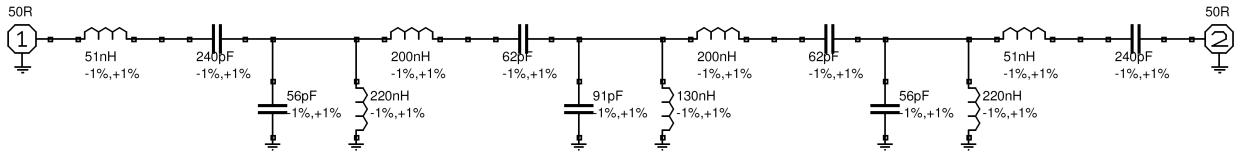


Figure 3: 10MHz - 80MHz, 7th-Order BPF Circuit

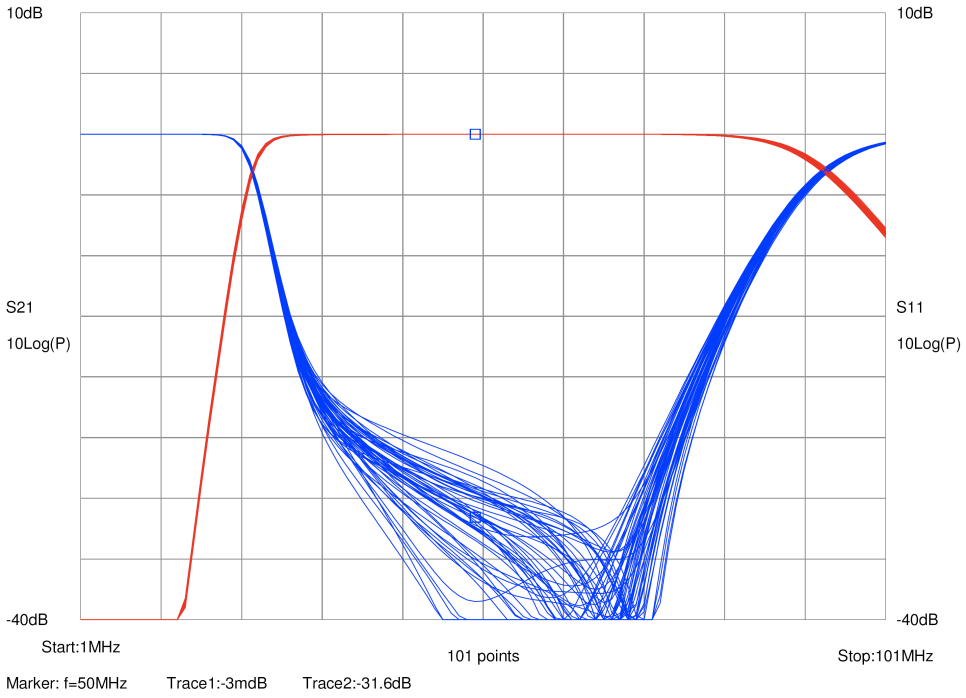


Figure 4: 10MHz - 80MHz, 7th-Order BPF S21 & S11

It is possible that multiple sections may need to be cascaded throughout the analog receiver to provide the required attenuation to mitigate out-of-band signals. A notch filter may be implemented to increase the amount of attenuation in the FM band. A notch filter design and cascaded performance with the highpass/lowpass filter is shown in section 4.

2. 28MHz - 54MHz Reduced-Bandwidth Filter

The reduced bandwidth filter can be designed with a resonant bandpass structure since the bandwidth is less than twice the high cutoff frequency. Figure 5 shows S21 for multiple orders of butterworth bandpass filters centered at 41MHz having 26MHz of bandwidth.

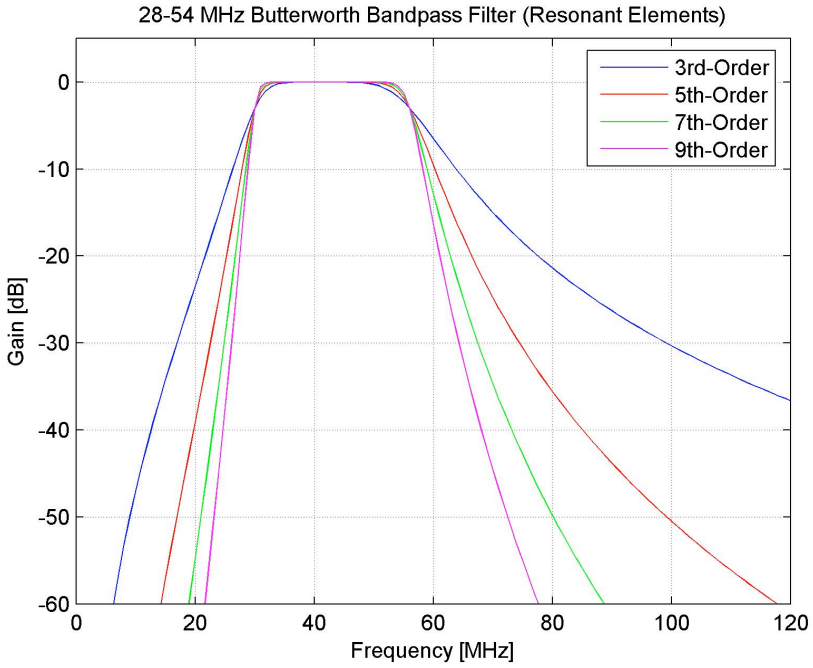


Figure 5: Insertion loss for multiple orders of 28-54MHz butterworth bandpass filters

Figure 6 shows the circuit elements for a 5th-Order BPF (41MHz center frequency, 26MHz bandwidth) using standard value components. This filter provides 30dB attenuation at 20MHz and 45dB attenuation at 90MHz. Return loss is better than 20dB over most the passband (Figure 7).

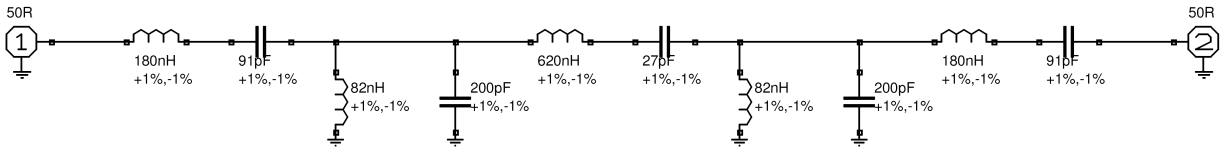


Figure 6: 28MHz - 54MHz, 5th-Order BPF Circuit

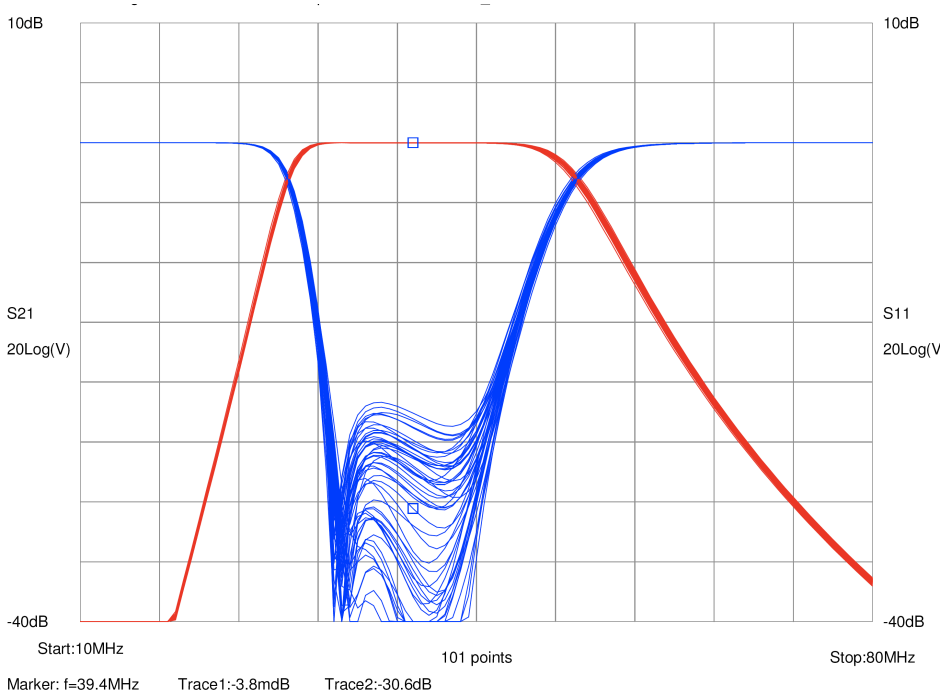


Figure 7: 28MHz - 54MHz, 7th-Order BPF S21 & S11

3. 41MHz Diplexer Low-Shelf Filter

The full bandwidth may be split with a diplexer circuit. As with any of these filters, dispersion at the band edges is a concern. When recombining the signals, a large increase in return loss is simulated. It is undetermined how much of an effect the actual circuit will have on the digitized bandwidth. A split frequency of 41MHz was chosen in case the center frequency exhibits too much dispersion to provide observable bandwidth. The center bandwidth will be observable from two other filter configurations as a means for checking the integrity of the diplexer configuration.

A digital step attenuator will be used to provide gain control over the low frequency portion of the bandwidth. Simulations of this configuration were implemented with pi-pad attenuators in place of the step attenuator. A 6th-Order diplexer low-shelf filter is shown in Figure 8. Simulations for 6dB down and 25dB down are shown in Figures 9 and 10. A 6th-Order diplexer was selected on the basis of providing adequate roll-off to attenuate the low-band RFI at the maximum attenuation of 25dB.

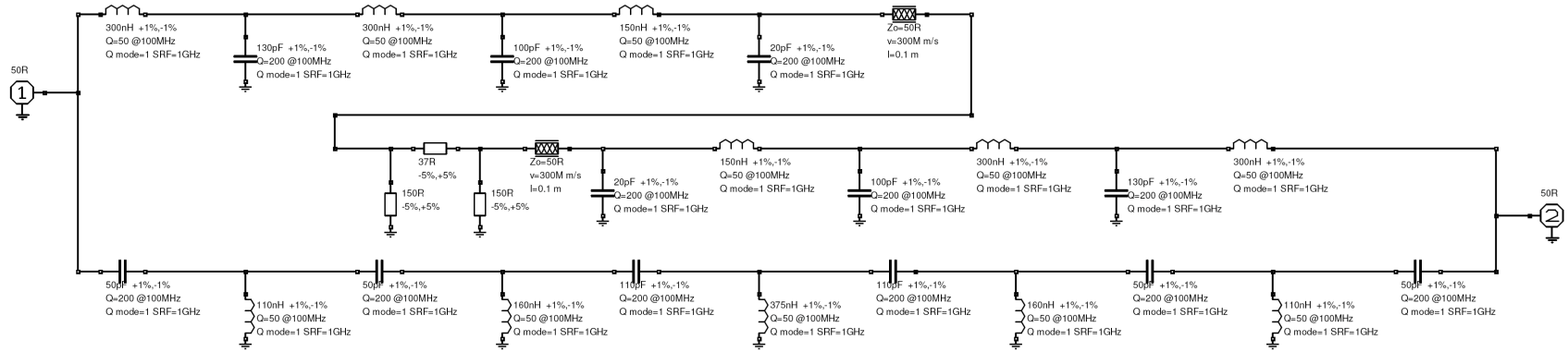


Figure 8: Diplexer Low-Shelf Filter

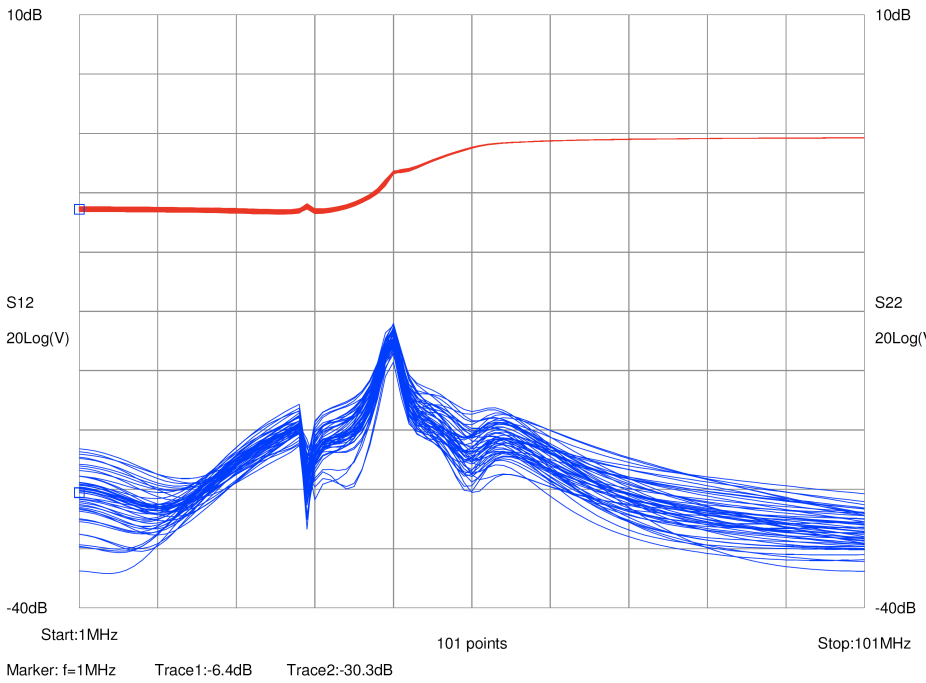


Figure 9: 6dB down low-shelf filter

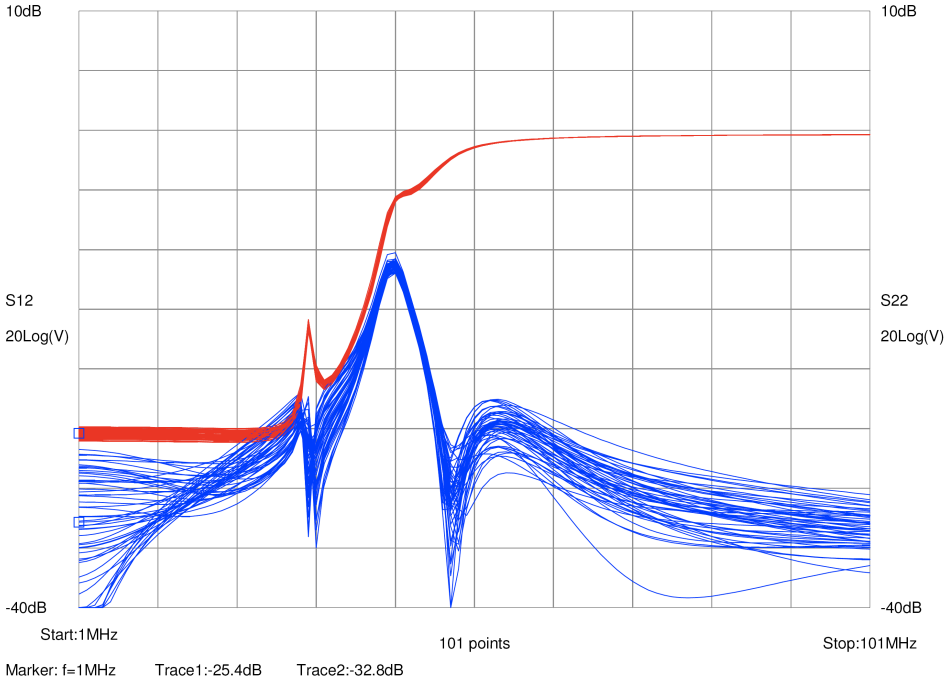


Figure 10: 25dB down low-shelf filter

4. 98MHz FM Band Notch Filter

It is possible that a separate filter will be required to attenuate the RFI in the FM band. A 3rd-Order notch filter (bandstop) is provided in Figure 11. The component values have been chosen to provide good passband performance when cascaded with the full-bandwidth filter (see Figure 16).

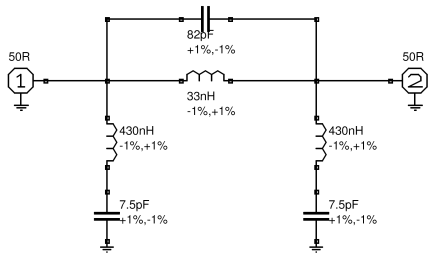


Figure 11: 3rd-Order FM notch filter

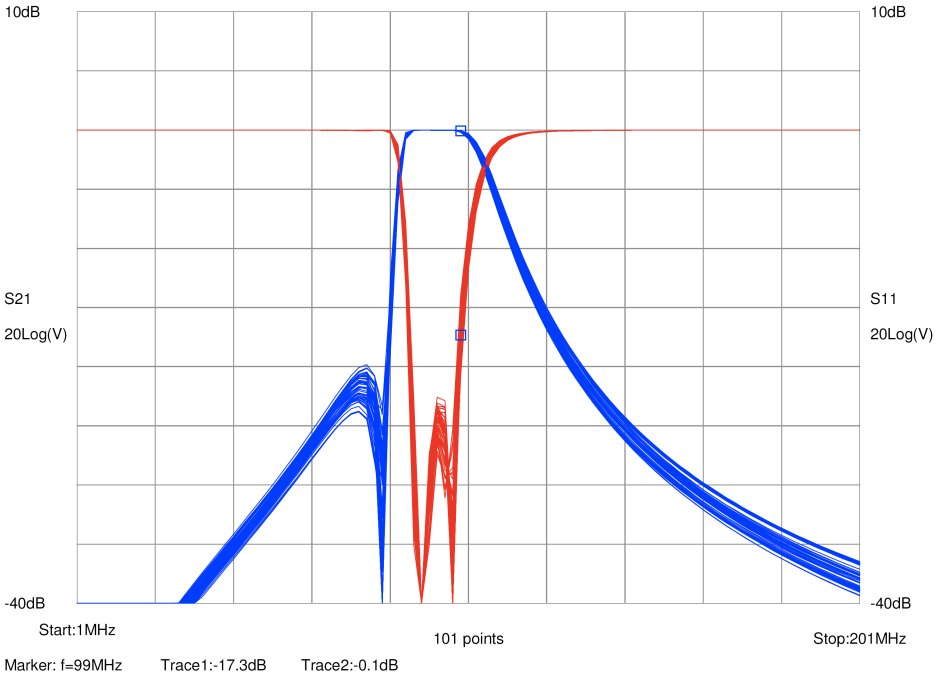


Figure 12: 98MHz FM notch filter S21 & S11

5. ARX Configuration Simulations

The full ARX frequency response simulations are provided for each possible configuration. Since the 10-80MHz filter will always be in the signal path, it is useful to analyze the results of cascading the 28-54MHz filter and low-shelf diplexer filter with the 10-80MHz filter. Figures 13-15 are good representations of the actual frequency response of the different configurations. Figure 16 shows the response of the 10-80MHz filter with the 98MHz FM notch filter.

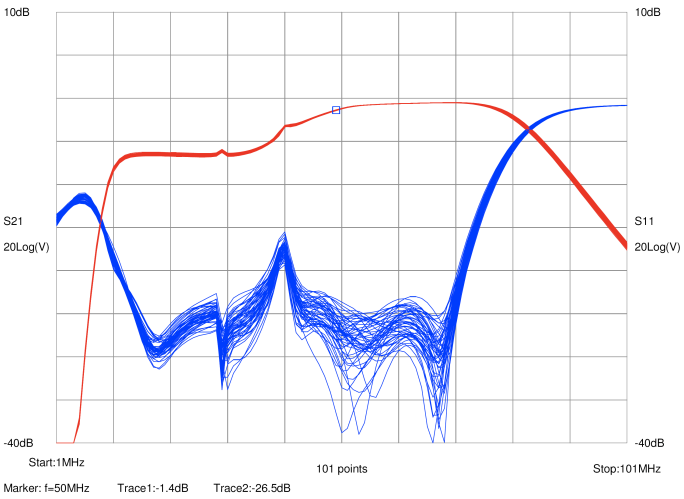


Figure 13: 6dB down low-shelf configuration

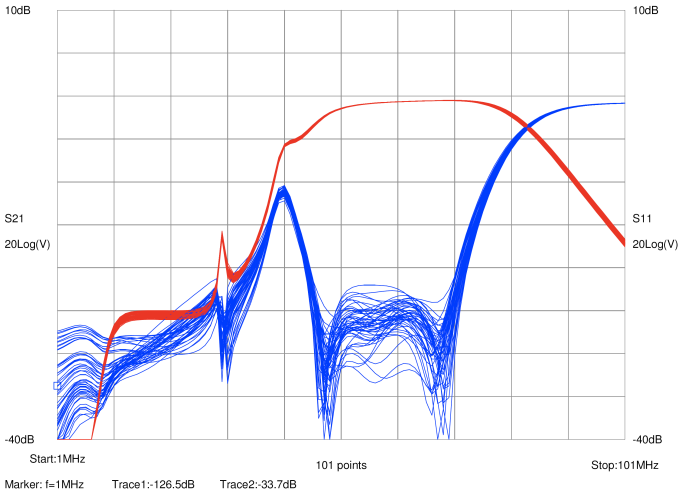


Figure 14: 25dB down low-shelf configuration

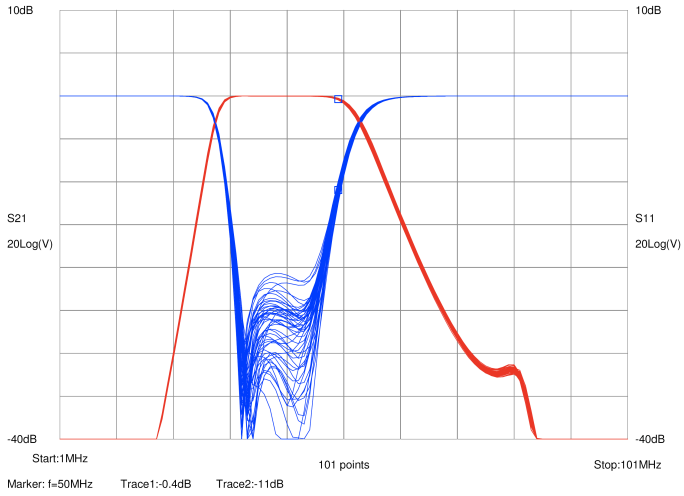


Figure 14: Reduced bandwidth configuration

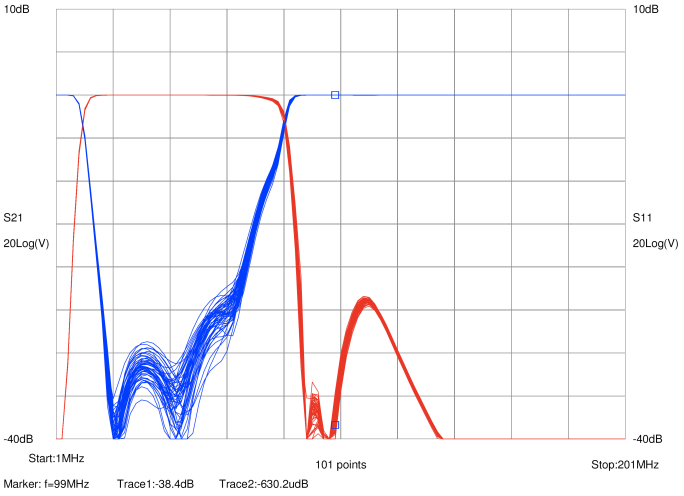


Figure 15: Full bandwidth configuration with notch filter

6. Filter Design Guide

Microwave LC ladder filter networks are usually designed by cookbook method and tuned for performance. This design guide details the steps necessary to modify any of the ARX filters and design new filters as needed. The first step in realizing a lumped element filter is to choose a prototype lowpass topology. The Pi Network starts with a shunt element, the Tee Network starts with a series elements (Figure 16). It is usually desirable to minimize the number of inductors required since the physical parameters are less ideal than capacitors. If a lowpass is being designed, no component changes are necessary. To transform the filter from a lowpass into highpass, replace all capacitors by inductors. The component replacements for bandpass and bandstop filters are given below. Table 1 gives the normalized doubly-terminated butterworth component values for various filter orders. Table 2 gives the component values for a singly-terminated filter. The singly-terminated table should be used when designing the diplexer. These values are the Farad capacitance and Henry inductance to design either Pi or Tee network filters for a 1 Hz cutoff frequency and 1 Ohm impedance. The next step is to scale the component values to the chosen cutoff frequency and load impedance. The scaling equations are given below. After ideal have been determined, replacing the values with standard values is required. Tuning is done by selecting standard values either higher or lower than the ideal values and simulating the circuit to determine the result.

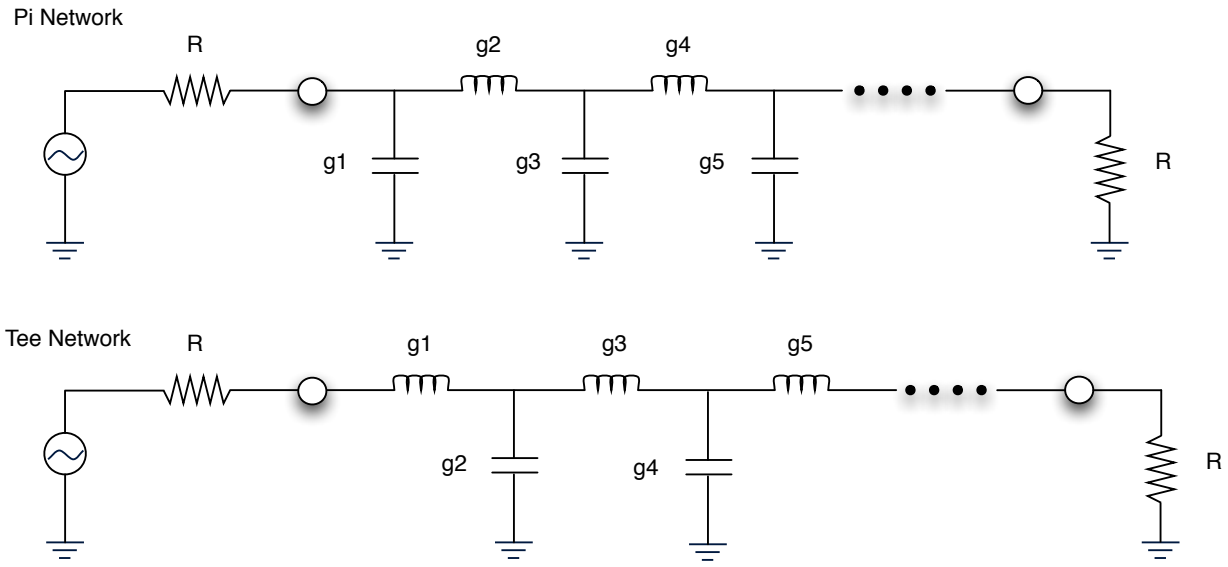


Figure 16: Doubly-Terminated Lowpass LC ladder filter topologies

Order	g1	g2	g3	g4	g5	g6	g7	g8	g9	g10
1	2.000									
2	1.414	1.414								
3	1.000	2.000	1.000							
4	0.764	1.848	1.848	0.764						
5	0.618	1.618	2.000	1.618	0.618					
6	0.518	1.414	1.932	1.932	1.414	0.518				
7	0.445	1.247	1.802	2.000	1.802	1.247	0.445			
8	0.390	1.111	1.663	1.962	1.962	1.663	1.111	0.390		
9	0.347	1.000	1.532	1.879	2.000	1.879	1.532	1.000	0.347	
10	0.313	0.908	1.414	1.782	1.975	1.975	1.782	1.414	0.908	0.313

Table 1: Doubly-Terminated Butterworth Lowpass Prototype Element Values

Order	g1	g2	g3	g4	g5	g6	g7	g8	g9	g10
1	1.000									
2	0.707	1.414								
3	0.500	1.333	1.500							
4	0.383	1.082	1.577	1.531						
5	0.309	0.8944	1.382	1.694	1.545					
6	0.259	0.758	1.202	1.553	1.759	1.553				
7	0.223	0.656	1.055	1.397	1.659	1.799	1.558			
8	0.195	0.578	0.937	1.259	1.528	1.729	1.825	1.561		
9	0.174	0.516	0.841	1.141	1.404	1.620	1.777	1.842	1.563	
10	0.156	0.465	0.763	1.041	1.292	1.510	1.687	1.812	1.855	1.564

Table 2: Singly-Terminated Butterworth Lowpass Prototype Element Values

Scaling Equations for component values given normalized g component values

Low-Pass (use prototype elements)	**High-Pass** (replace prototype element with opposite)
$L = \frac{g_x \cdot R}{2 \cdot \pi \cdot f_c}$	$L = \frac{R}{2 \cdot \pi \cdot f_c \cdot g_x}$
$C = \frac{g_x}{2 \cdot \pi \cdot f_c \cdot R}$	$C = \frac{1}{2 \cdot \pi \cdot f_c \cdot R \cdot g_x}$

Bandpass (transform using upper cutoff frequency and lower cutoff frequency of filter):

Replace each capacitor with a parallel capacitor and inductor network.

$$C = \frac{g_x}{2 \cdot \pi \cdot (F_u - F_l) \cdot R}$$

$$L = \frac{(F_u - F_l) \cdot R}{2 \cdot \pi \cdot F_u \cdot F_l \cdot g_x}$$

Replace each inductor with a series capacitor and inductor network.

$$C = \frac{F_u - F_l}{2 \cdot \pi \cdot F_u \cdot F_l \cdot R \cdot g_x}$$

$$L = \frac{R \cdot g_x}{2 \cdot \pi \cdot (F_u - F_l)}$$

Bandstop (transform using upper cutoff frequency and lower cutoff frequency of filter):

Replace each capacitor with a series capacitor and inductor network.

$$C = \frac{1}{2 \cdot \pi \cdot (F_u - Fl) \cdot R \cdot g_x}$$

$$L = \frac{(F_u - F_l) \cdot R \cdot g_x}{2 \cdot \pi \cdot F_u \cdot F_l \cdot}$$

Replace each inductor with a parallel capacitor and inductor network.

$$C = \frac{(F_u - F_l) \cdot g_x}{2 \cdot \pi \cdot F_u \cdot F_l \cdot R}$$

$$L = \frac{R}{2 \cdot \pi \cdot (F_u - F_l) \cdot g_x}$$

References:

[1] Gabor C. Temes and Sanjit K. Mitra, *Modern Filter Theory and Design,* John Wiley & Sons, 1973

[2] Erich Cristian, *LC-FILTERS Design, Testing and Manufacturing,* John Wiley & Sons, 1983

[3] Arthur B. Williams, *Electronic Filter Design Handbook,* McGraw-Hill, 1981

[4] Kendall L. Su, *Analog Filters,* Chapman & Hall, 1996

[5] Steve Winder, *Filter Design*, Newnes, 1997

[6] George L. Matthaei, Leo Young, E. M. T. Jones, *Microwave Filters, Impedance-Matching Networks, and Coupling Structures*, McGraw-Hill, 1964

LWA Engineering Memo

Brassboard Analog Receiver Schematic

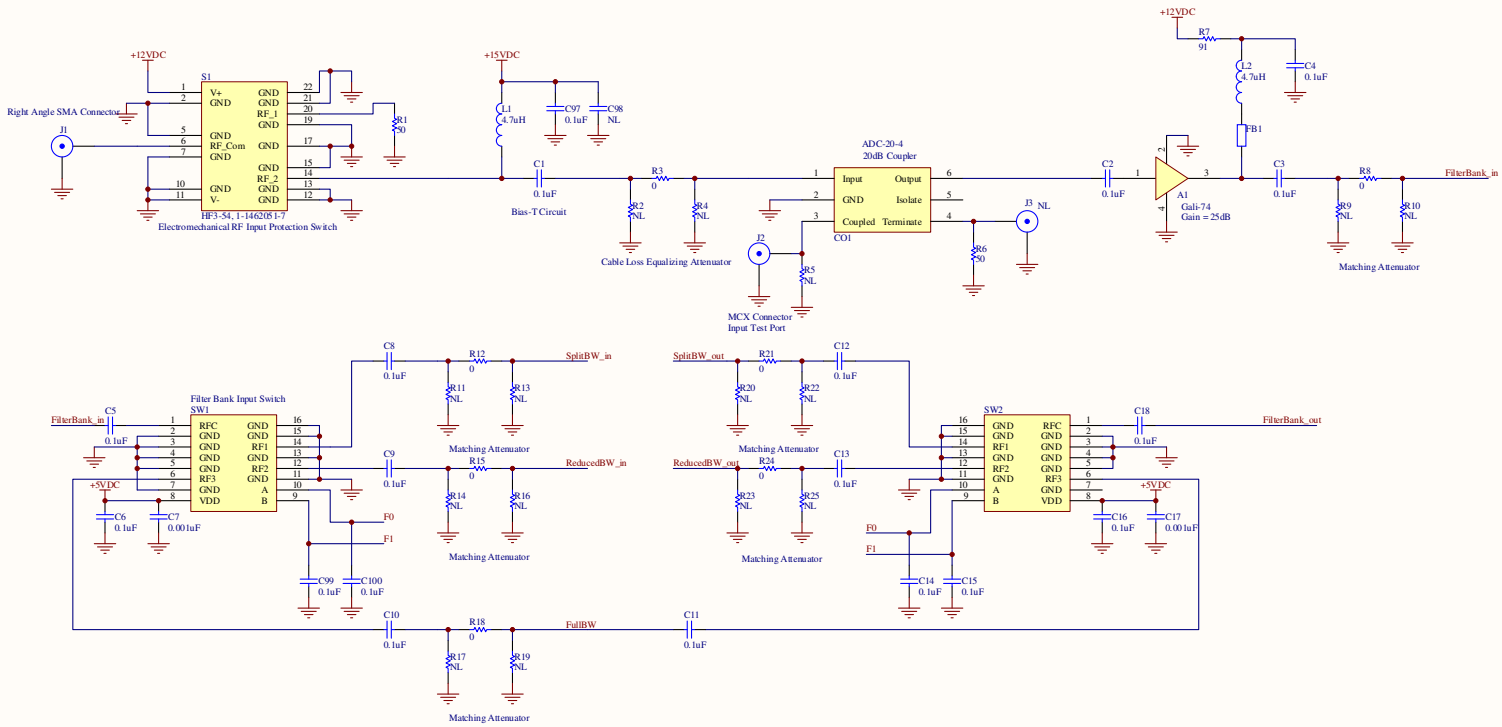
Task: ARX0007
Joe Craig
June 6, 2008

A brassboard ARX module will be designed to facilitate receiver testing and prototyping. The module will provide two to four receive channels, depending on the mechanical packaging of the chosen. The generalized block diagram for each receive channel is given in ARX0004A. The schematic provided illustrates a single receive channel, power regulation and control logic circuitry. The receive channel will be duplicated as many times as the physical board space allows, but no less than two channels so that channel-to-channel coupling can be measured. It is the intention to control the settings of the brassboard ARX (gain, filter, etc.) by an external logic controller via a 25 pin DSub connector. RF inputs, outputs and coupled test points will be provided via SMA and MCX connectors. The module will accept a single supply voltage of +18VDC. Many test points and 'no-load' footprints are provided to facilitate prototyping modifications and testing. A complete bill-of-materials has not yet been generated as there are still some component that need to be selected such as capacitors and inductors, although the appropriate values are shown in the schematic.

The brassboard will provide the following features:

1) Bias-T for powering FEE
   - Each channel will have it's own +15VDC regulator with a logic on/off bit
2) Reconfigurable Filters
   - Three filter selections will be possible via two logic control bits. A full-bandwidth filter, a reduced bandwidth filter, and a split bandwidth filter with gain control. A resonant element FM notch filter is also included.
3) Gain Control
   - A possible maximum gain of 75dB will be provided with a possible 60dB of attenuation control.

The diplexer (split bandwidth) circuit introduces the most risk and some additional footprints for prototyping may be included to test the options of resistively combining the spit bandwidths instead of using a reverse diplexer to combine the two bandwidths. The +15VDC regulator for powering the FEEs includes an on/off control bit. The Sharp PQ15R15 is the only regulator sourced which provides the voltage/ current required and has an on/off control bit. This part is discontinued and it is likely that the final ARX design must include a power MOSFET (or similar circuit) to turn FEE power on and off. The ARX module will accept 5V TTL/CMOS logic signals and buffer them to +3V where needed. Pull-up/down resistors are proved to default the ARX configuration to full-bandwidth and max. gain when used without an external logic controller.



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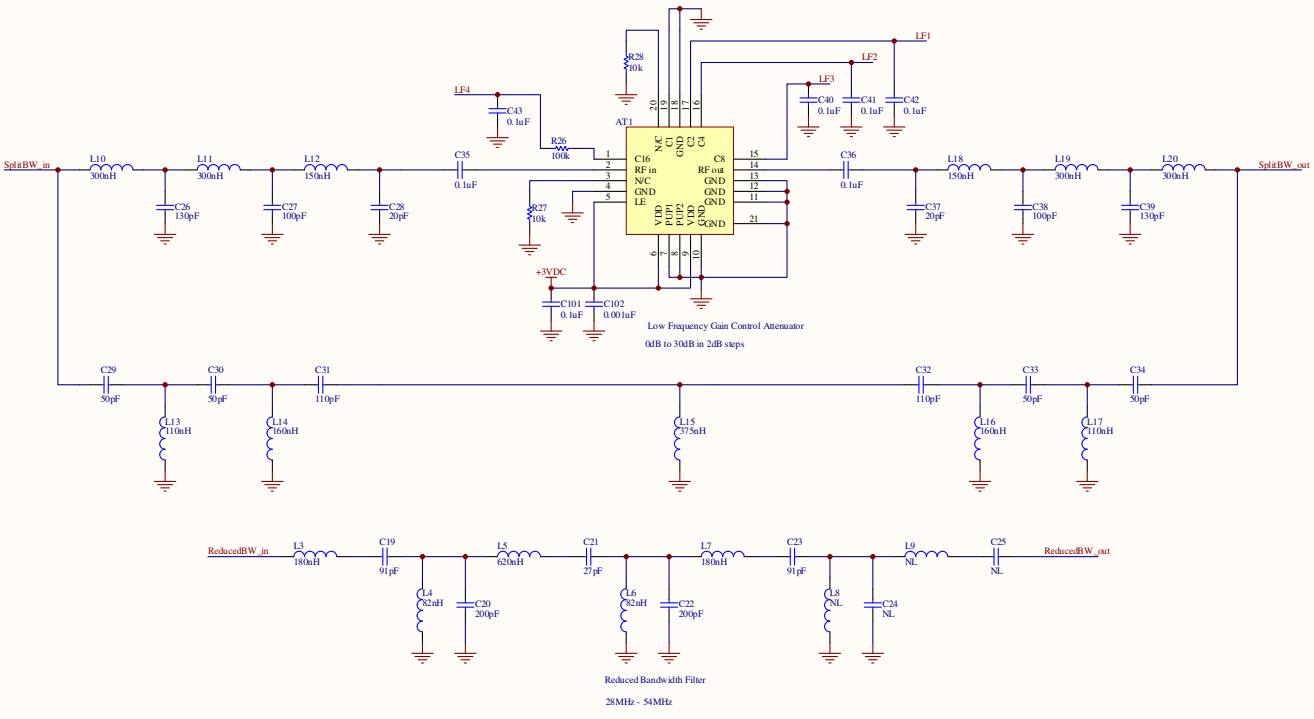

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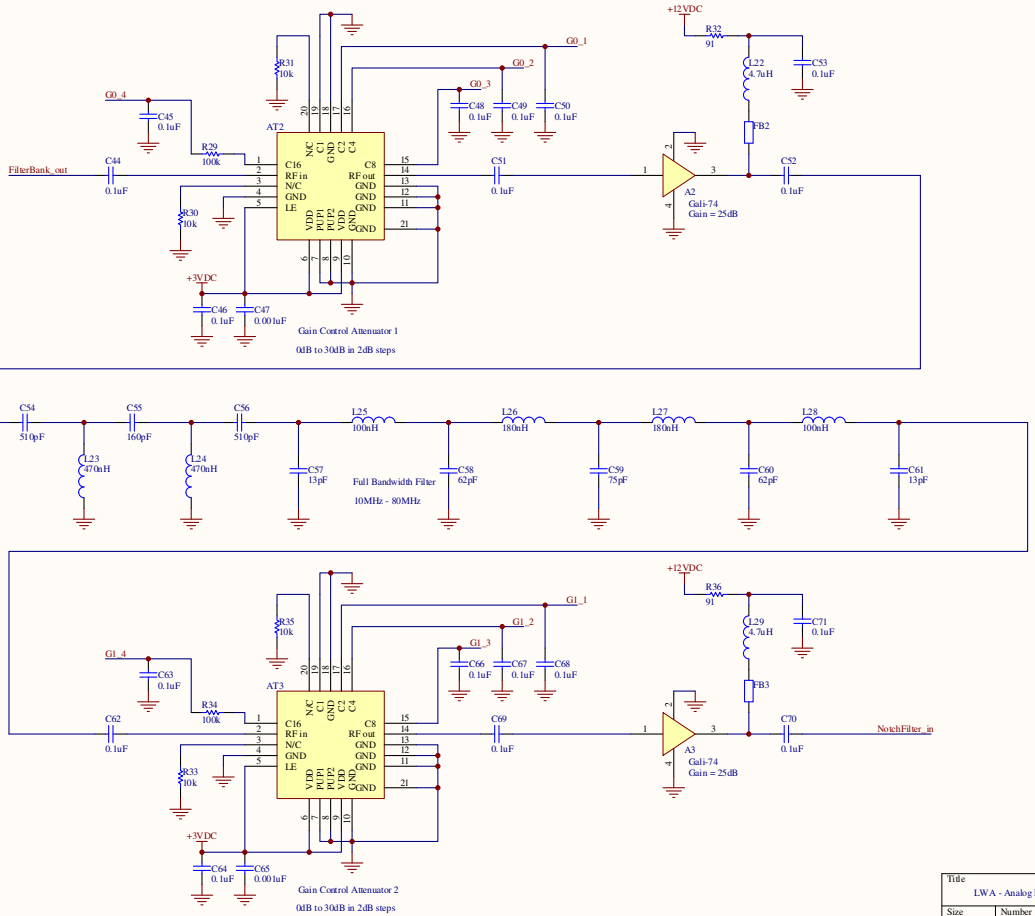

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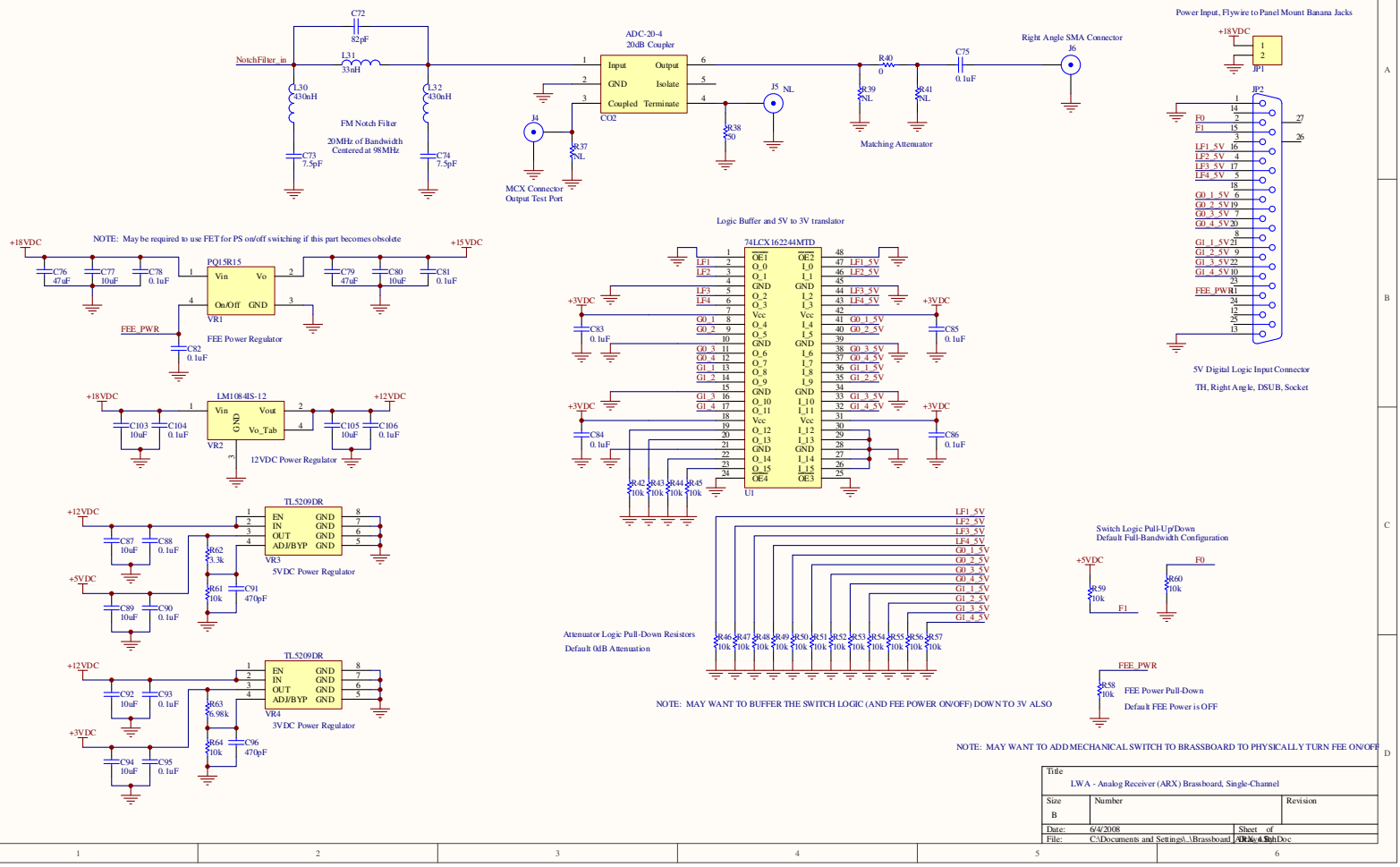

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LWA Engineering Memo

ARX Requirements v1

Task: ARX0008
Joe Craig
June 13, 2008

This document is an initial set of requirements for the LWA analog receiver. The requirements are broken down by filter configuration. Many metrics are TBD and are provided as a means of identifying critical parameters. ARX module requirements are not included, but should be determined for future requirements documentation.

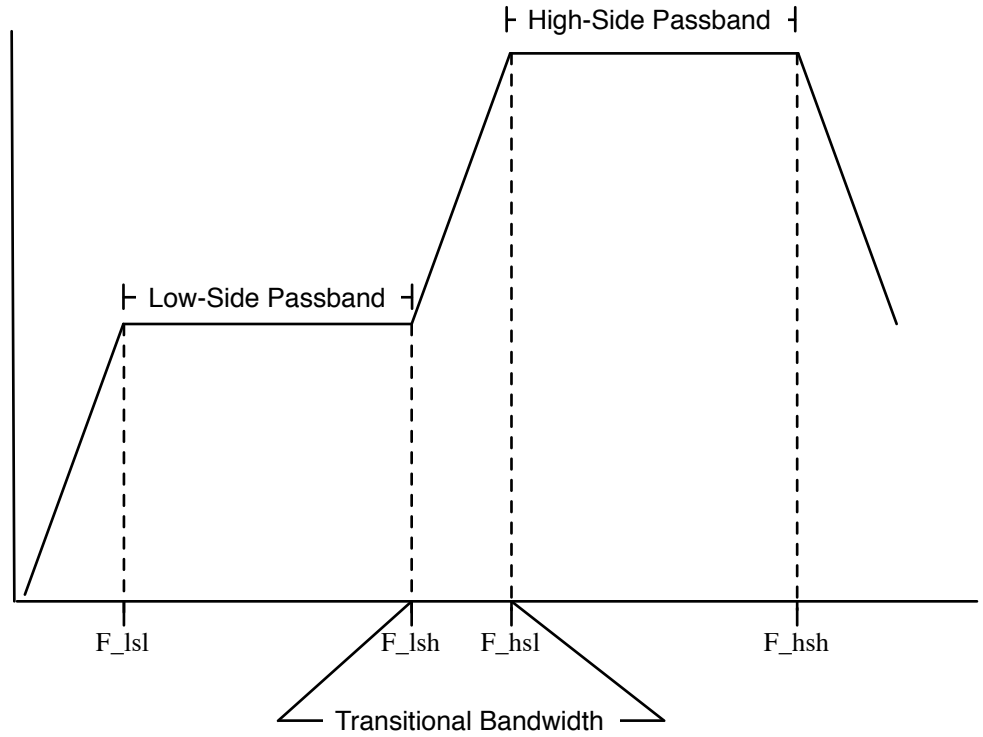
1. Filter Configuration 1: Full-Bandwidth

ARX Parameter	Requirement
3dB Bandwidth	70MHz, +/- 3MHz
Low-Side 3dB Cutoff Frequency	10MHz, +/- 1MHz
High-Side 3dB Cutoff Frequency	80MHz, +/- 2MHz
Attenuation at 3MHz	$\geq$ 50dB
Attenuation at 88MHz	$\geq$ 35dB
Passband Max. VSWR	TBD
Max. Gain	65dB, +/- TBD
Min. Gain	5dB, +/- TBD
Gain Control Steps	2dB, +/- 1dB
Linearity: IP1dB (Min. Gain)	$\geq$ -17dBm
Linearity: IP1dB (Max. Gain)	$\geq$ -62dBm
Linearity: IIP3 (Min. Gain)	$\geq$ -2dBm
Linearity: IIP3 (Max. Gain)	$\geq$ -47dBm
Noise Figure (Min. Gain)	$\leq$ TBD
Noise Figure (Max. Gain)	$\leq$ 7dB

2. **Filter Configuration 2: Reduced Bandwidth**

ARX Parameter	Requirement
3dB Bandwidth	26MHz, +/- 2MHz
Low-Side 3dB Cutoff	28MHz, +/- 1MHz
High-Side 3dB Cutoff	54MHz, +/- 1MHz
Attenuation at 3MHz	$\geq$ 100dB
Attenuation at 88MHz	$\geq$ 80dB
Passband Max. VSWR	TBD
Max. Gain	65dB, +/- TBD
Min. Gain	5dB, +/- TBD
Gain Control Steps	2dB, +/- 1dB
Linearity: IP1dB (Min. Gain)	$\geq$ -17dBm
Linearity: IP1dB (Max. Gain)	$\geq$ -62dBm
Linearity: IIP3 (Min. Gain)	$\geq$ -2dBm
Linearity: IIP3 (Max. Gain)	$\geq$ -47dBm
Noise Figure (Min. Gain)	$\leq$ TBD
Noise Figure (Max. Gain)	$\leq$ 7dB

3. **Filter Configuration 3: Split-Bandwidth**



ARX Parameter	Requirement
Low-Side Low Cutoff Frequency (F_lsl)	10MHz, +/- 1MHz
Low-Side High Cutoff Frequency (F_lsh)	30MHz, +/- 6MHz
Transitional Bandwidth (F_hsl - F_lsh) @ 6dB down	20MHz, +/- 2MHz
Transitional Bandwidth (F_hsl - F_lsh) @ 25dB down	23MHz, +/- 2MHz
High-Side Low Cutoff Frequency (F_hsl)	50MHz, +/- 1MHz
High-Side High Cutoff Frequency (F_hsh)	80MHz, +/- 2MHz
Attenuation at 3MHz	$\geq$ 55dB
Attenuation at 88MHz	$\geq$ 35dB
Low-Side Passband Max. VSWR	TBD
High-Side Passband Max. VSWR	TBD
Low-Side Passband Max. Gain	65dB, +/- TBD

ARX Parameter	Requirement
Low-Side Passband Min. Gain	-20dB, +/- TBD
Low-Side Gain Control Steps	2dB, +/- 1dB
High-Side Passband Max. Gain	65dB, +/- TBD
High-Side Passband Min. Gain	5dB, +/- TBD
High-Side Gain Control Steps	2dB, +/- 1dB
Low-Side Linearity: IP1dB (Min. Gain)	$\geq$ +8dBm
Low-Side Linearity: IP1dB (Max. Gain)	$\geq$ -62dBm
Low-Side Linearity: IIP3 (Min. Gain)	$\geq$ +23dBm
Low-Side Linearity: IIP3 (Max. Gain)	$\geq$ -47dBm
Low-Side Noise Figure (Min. Gain)	$\leq$ TBD
Low-Side Noise Figure (Max. Gain)	$\leq$ 7dB
High-Side Linearity: IP1dB (Min. Gain)	$\geq$ -17dBm
High-Side Linearity: IP1dB (Max. Gain)	$\geq$ -62dBm
High-Side Linearity: IIP3 (Min. Gain)	$\geq$ -2dBm
High-Side Linearity: IIP3 (Max. Gain)	$\geq$ -47dBm
High-Side Noise Figure (Min. Gain)	$\leq$ TBD
High-Side Noise Figure (Max. Gain)	$\leq$ 7dB

LWA Engineering Memo

ARX Brassboard Constraints and Packaging

Task: ARX0009
Joe Craig
June 28, 2008

Provided below are the details for the Analog Receiver's Brassboard PCB size constraints based on the initially chosen mechanical packaging.

The Vector Electronics EFP Series Modules (Figure 1) has been identified for ease-of-use, cost-effectiveness, and appropriate size constraints. The CMA Series rack unit (Figure 2) can house up to 8 EFP modules. The PCB slides into the modules on fingers and can accommodate circuit boards of sizes 4.5" x 9.6" or 4.5" x 6.5" (depending on which module length is used).

The analog receiver board, sized by 4.5" x 9.6", can accommodate up to 4 receive chain channels (Figure 3). With 4 channels per module and 8 modules per rack; each 3U rack space could contain 32 channels in this prototype configuration. 512 channels would require 48U rack space, plus power supplies (42U is the standard space in a 19" full-size rack).

The important design details from the EFP Modules are listed below.

Orderable Part Number: EFP204A97(F)
Fits 4.5" x 9.6" PCB
Fits Board Thickness less than 0.076" (0.062" design thickness)
Distributor is Mouser Electronics, P/N: 574-EFP204A97F
Price $47.37 for quantities less than 10
Datasheet: http://www.vectorelect.com/Catpdf/Page%2045-46.pdf

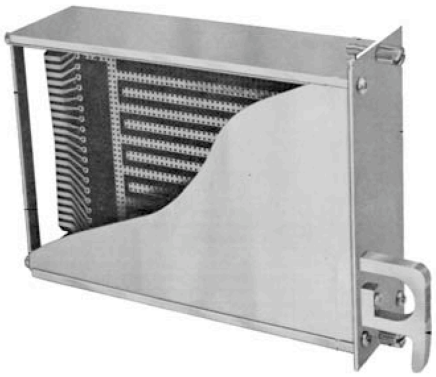


Figure 1: Vector EFP Series Module

Figure 2: Vector Electronics CMA Series Rack/Module Housing

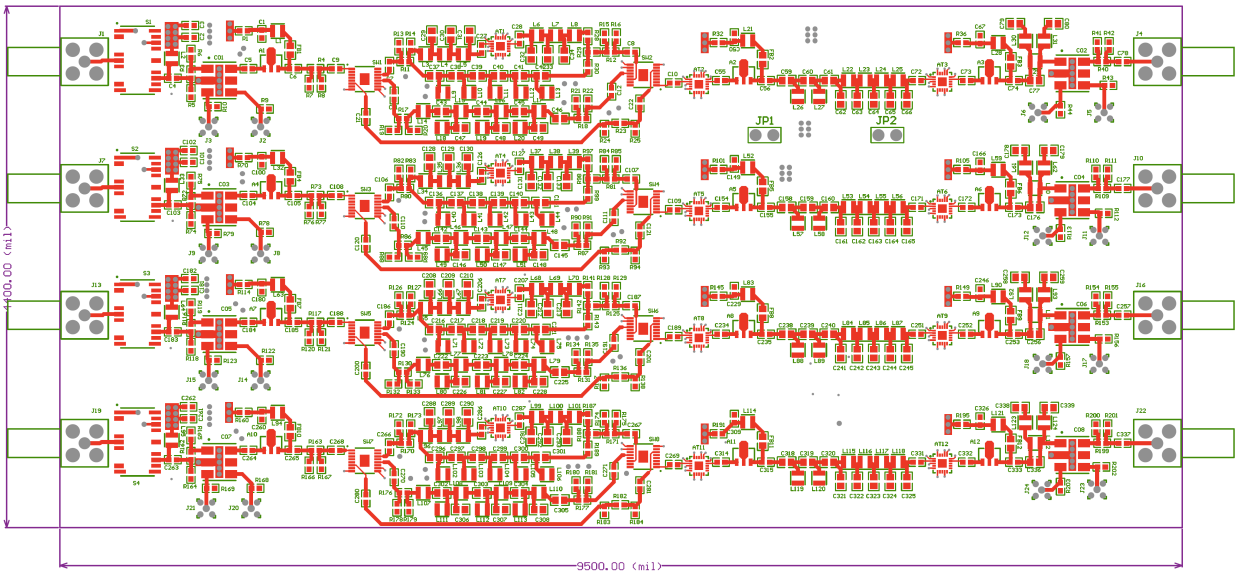


Figure 3: 4 Receive Channels using 4.5” x 9.6” PCB Size

LWA Engineering Memo

ARX Brassboard Digital Control and Power

Task: ARX0010
Joe Craig
June 29, 2008

A digital logic interface for controlling the gains, filter configurations, and power to the Front-End Electronics (FEE) is provided in the Brassboard Analog Receiver. 5V TTL/CMOS logic levels are used and buffered on the receiver board. A pin-out diagram is shown in Figure 1 for the receiver's logic interface connector. The signal functions are detailed in Table 1. A logical truth-table for filter configurations and attenuation steps are shown in Table 2 and Table 3 respectively.

Power is fed to the receiver module from two main supply lines; +15VDC (JP1) for powering the FEE and a +8VDC (JP2) for powering the receiver amplifiers and receiver components. Exact current draw specifications will be defined from testing.

Although any 5V TTL/CMOS logic controller can be used, a simple USB digital I/O controller from National Instruments (Figure 2) has been identified as an efficient solution to controlling the Brassboard Analog Receiver module with software (programmed in LabVIEW).

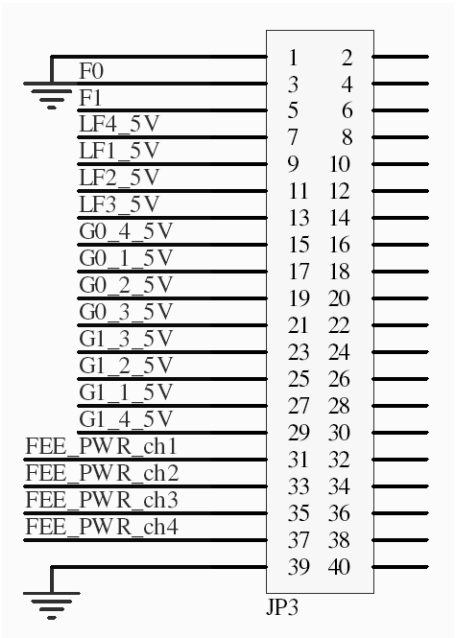


Figure 1: ARX Brassboard Digital Logic Connection Schematic

JP3 Pin	Signal Name	Function
1	GND	Logic Ground
3	F0	Filter Configuration - Bit 0
5	F1	Filter Configuration - Bit 1
7	LF4_5V	Low-Frequency Attenuator - Bit 4
9	LF1_5V	Low-Frequency Attenuator - Bit 1
11	LF2_5V	Low-Frequency Attenuator - Bit 2
13	LF3_5V	Low-Frequency Attenuator - Bit 3
15	G0_4_5V	First Attenuator - Bit 4
17	G0_1_5V	First Attenuator - Bit 1
19	G0_2_5V	First Attenuator - Bit 2
21	G0_3_5V	First Attenuator - Bit 3
23	G1_3_5V	Second Attenuator - Bit 3
25	G1_2_5V	Second Attenuator - Bit 2
27	G1_1_5V	Second Attenuator - Bit 1
29	G1_4_5V	Second Attenuator - Bit 4
31	FEE_PWR_ch1	FEE Power On/OFF - Channel 1 (ON = High)
33	FEE_PWR_ch2	FEE Power On/OFF - Channel 2 (ON = High)
35	FEE_PWR_ch3	FEE Power On/OFF - Channel 3 (ON = High)
37	FEE_PWR_ch4	FEE Power On/OFF - Channel 4 (ON = High)
39	GND	Logic Ground

Table 1: ARX Brassboard Logic Signals and Function

F0	F1	Filter State
Low	Low	Split-Bandwidth Filter Configuration
Low	High	Full-Bandwidth Filter Configuration
High	Low	Reduced Bandwidth Filter Configuration
High	High	Signal Chain OFF

Table 2: Filter Configuration Logical Truth-Table

Bit 4	Bit 3	Bit 2	Bit 1	Attenuation State
Low	Low	Low	Low	0 dB
Low	Low	Low	High	2 dB
Low	Low	High	Low	4 dB
Low	Low	High	High	6 dB
Low	High	Low	Low	8 dB
Low	High	Low	High	10 dB
Low	High	High	Low	12 dB
Low	High	High	High	14 dB
High	Low	Low	Low	16 dB
High	Low	Low	High	18 dB
High	Low	High	Low	20 dB
High	Low	High	High	22 dB
High	High	Low	Low	24 dB
High	High	Low	High	26 dB
High	High	High	Low	28 dB
High	High	High	High	30 dB

Table 3: Attenuation Logical Truth-Table

Figure 2: NI USB 6501 Digital I/O Controller

Information on the NI USB 6501
24 digital I/O lines, one 32-bit counter
5V TTL/CMOS Level, 8.5mA Current Drive
Built-in screw terminals for connectivity
USB 2.0 full-speed
Bus-powered design
Datasheet: http://www.ni.com/pdf/products/us/20054920301101dlr.pdf
National Instrument Part Number: 779205-01
Price: $99

LWA Engineering Memo

Laboratory Measurements of the Brassboard ARX

Task: ARX0014
Joe Craig, Steve Ellingson
Oct. 9, 2008

Version 2 of the LWA Brassboard Analog Receiver was tested thoroughly in the lab. This document presents the results of lab testing.

1. Magnitude Response

Figure 1 shows the gain of the receiver over frequency for three filter configurations. The Split Bandwidth configuration was set to 10 dB down. It is interesting to note the amount of selectivity which is achieved by cascading the resonant BPF structure in the Reduced Bandwidth configuration. The FM Notch filter does not seem to centered up correctly and will require some tuning/optimization. The Split Bandwidth configuration also needs some tuning as some resonance can be seen in the magnitude around 31 MHz and 40 MHz. The cascaded LP and HP filters in the Full Bandwidth configuration seem well behaved, but additional selectivity past the FM Notch may still be required. The maximum gain of the receiver is about 68 dB, which meets the requirements as stated in [1].

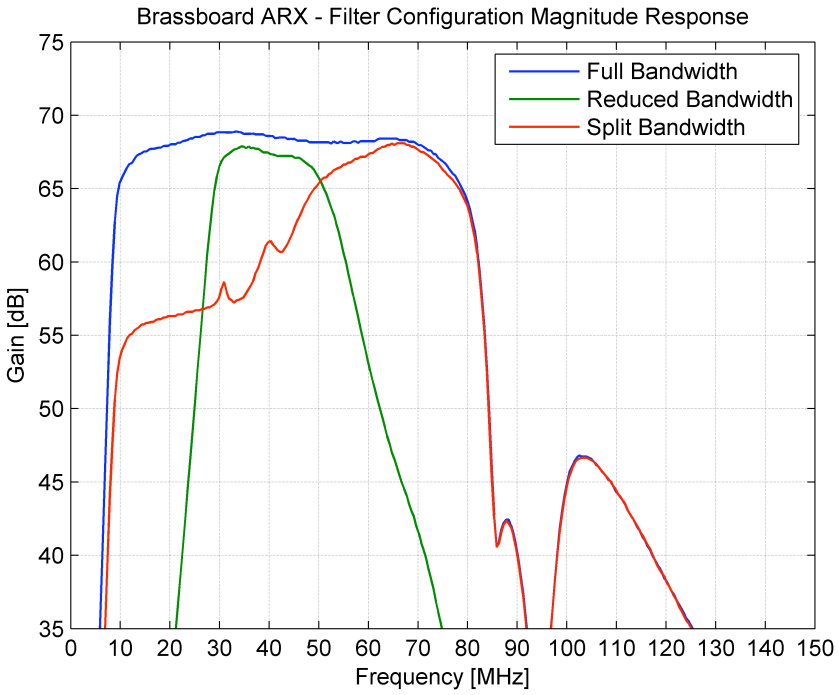


Figure 1: Magnitude Response of the 3 ARX filter configurations

2. Passband Magnitude and Phase Response

It is important to check the characteristics of the passband for each filter configuration. The magnitude (gain) and phase (group delay) is shown below for each filter configuration.

2.1 Full Bandwidth Filter Configuration

The Full Bandwidth configuration (Figure 2) was designed for 10 MHz and 80 MHz cutoff frequencies (-3 dB points). The passband ripple appears to be ~1dB over the range of 20 MHz to 70 MHz. The phase appears fairly linear and dispersion is not very apparent until the frequencies approach the band edges.

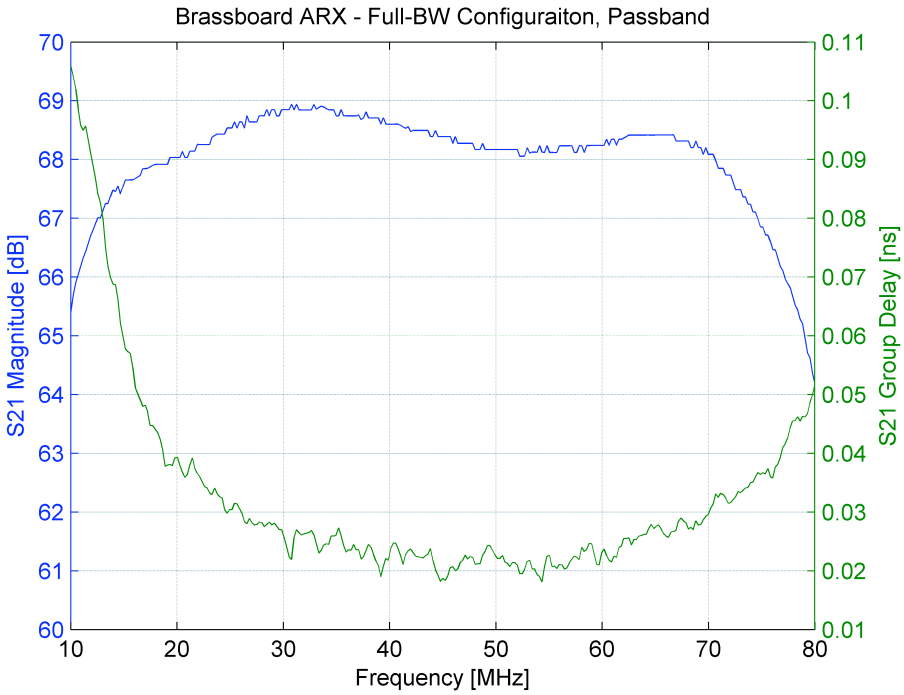


Figure 2: Full Bandwidth Filter Configuration, Passband 10 MHz - 80 MHz, Magnitude and Delay Measurement

2.2 Reduced Bandwidth Filter Configuration

The Reduced Bandwidth configuration (Figure 3) was design for 28 MHz to 54 MHz -3dB points. There appears to be ~1dB of ripple over 30 MHz to ~47 MHz. The phase response in this configurations shows slight dispersive ripples through the passband. This may, just as likely, be test equipment sensitivity as the DUT. The dispersion is probably insignificant for calibration.

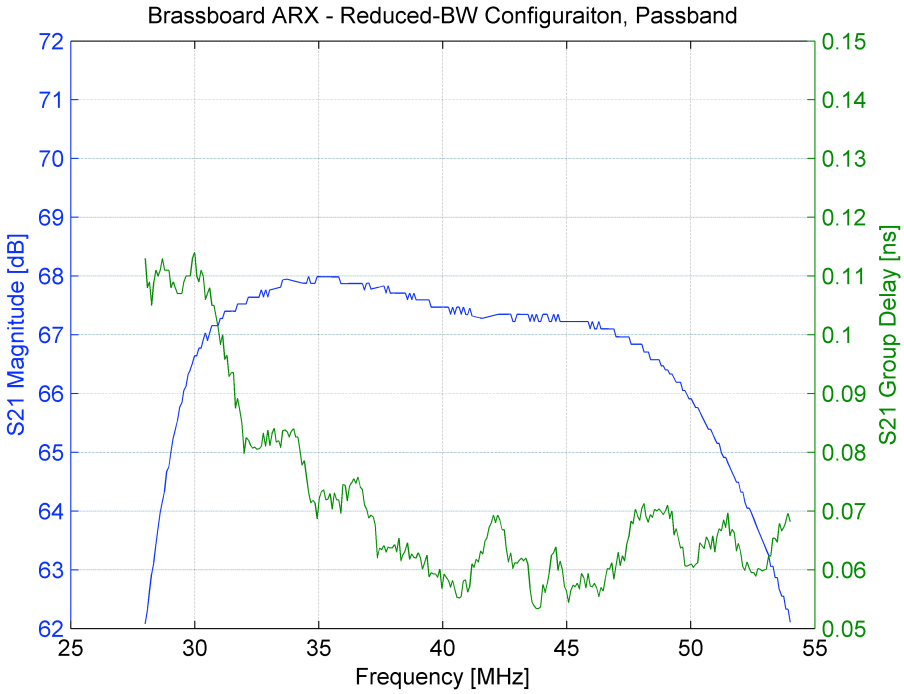


Figure 3: Reduced Bandwidth Filter Configuration, Passband 28 MHz - 54 MHz, Magnitude and Delay Measurement

2.3 Split Bandwidth Filter Configuration

The Split Bandwidth configuration (Figure 4), although functional, will require a significant amount of tuning to optimize the diplexer impedances. Magnitude resonances are seen at 31 MHz and 40 MHz. These resonances increase in magnitude at greater low-frequency attenuations. Although the dispersion appears slightly problematic at the crossover frequency (42 MHz), the rest of the passband appears fairly phase stable. The band-edge below 15 MHz (as also identified in the full bandwidth configuration), should be investigated.

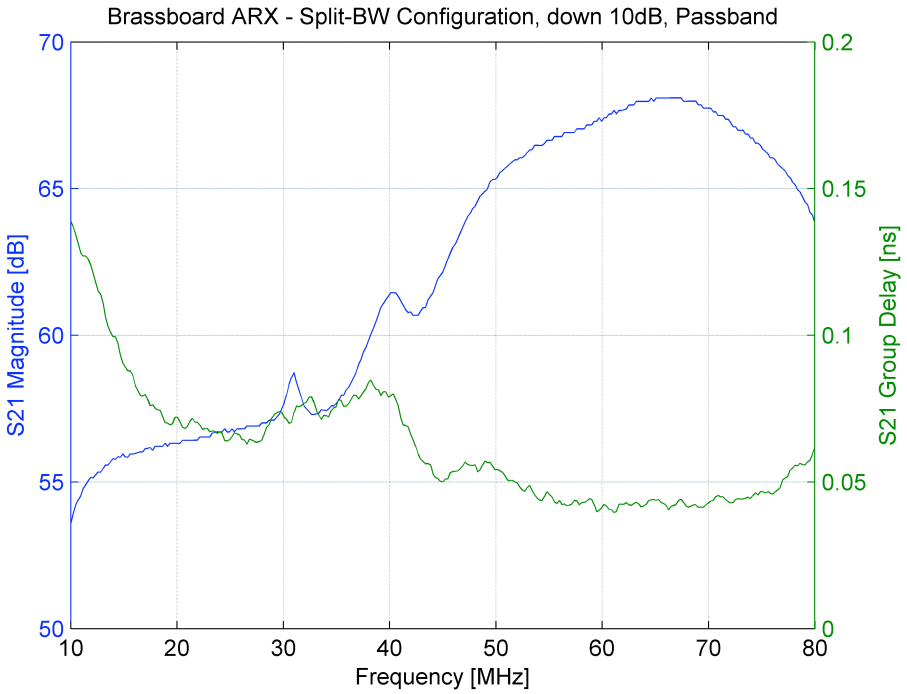


Figure 4: Split Bandwidth Filter Configuration, down by 10 dB, Passband 10 MHz - 80 MHz, Magnitude and Delay Measurement

3. Input Impedance & VSWR

The S11 complex impedance was measured using the FSH3 spectrum analyzer with VSWR bridge. The input impedance is shown in Figure 5. The match is very good at 80 MHz, but gets poor down towards 10 MHz. The VSWR is plotted in Figure 6. The cause of impedance mismatch towards the low-frequencies should be investigated.

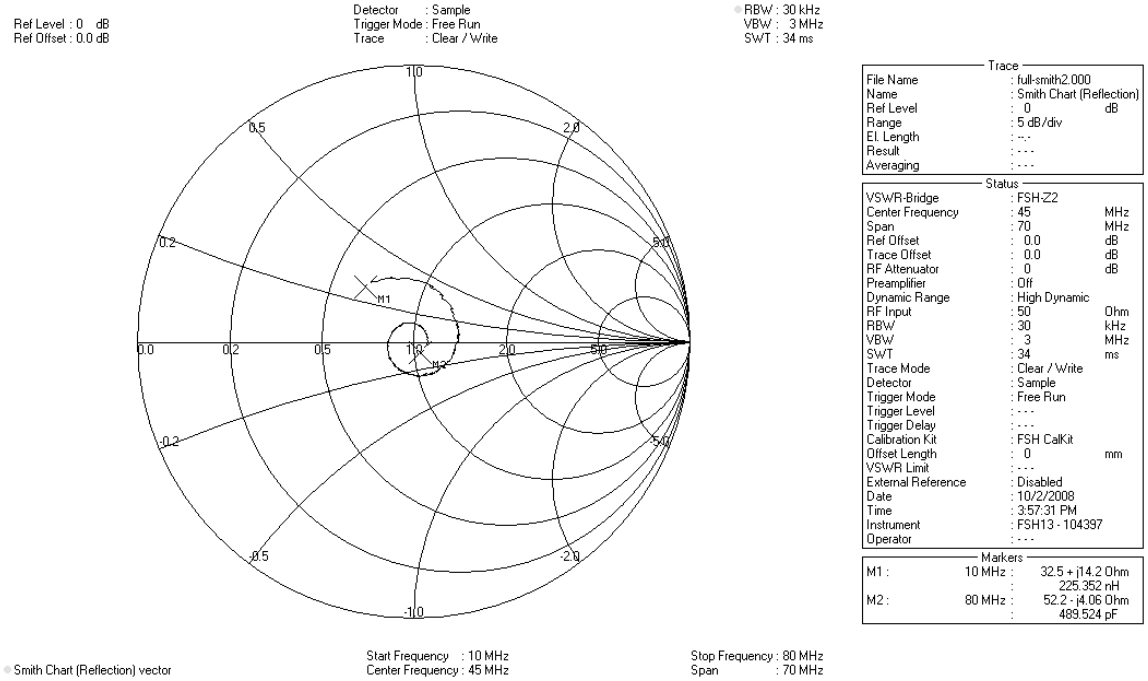


Figure 5: Measured Complex Impedance, S11 Reflection

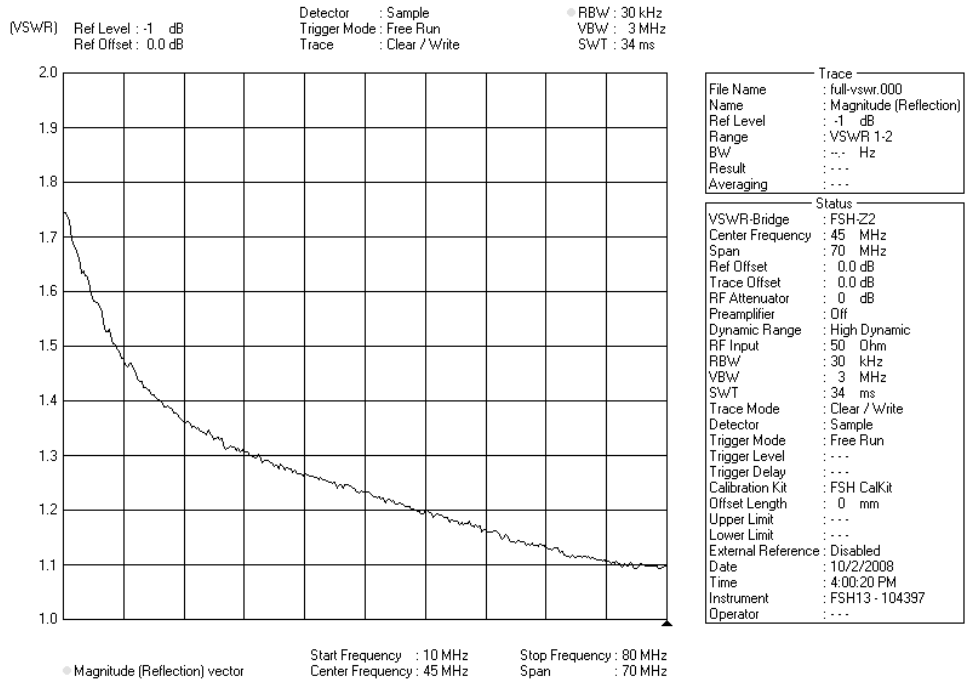


Figure 6: Measured VSWR, S11 Reflection

4. IP1dB & IIP3 Linearity

The receiver linearity is measured in terms of IP1dB and IIP3. The full-bandwidth filter configuration was used at the maximum receiver gain setting. IP1dB was measured with a test-tone at 70 MHz. IIP3 was measured using the two-tone setup (Figure 7), tones at 70 MHz and 71 MHz. The third-order products exist at 69 MHz and 71 MHz. For every 1 dB increase in signal power, the third-order products should increase by 3 dB. Figure 8 shows the data taken verifying the third-order slope is 3:1. IIP3 point is where the third-order linear curve intersects with the first-order linear curve. It should be approximately 10 dB higher than IP1dB. These linearity results meet the requirements stated in [1]. It will also be useful to measure the linearity as a function of frequency, filter configuration, and gain settings.

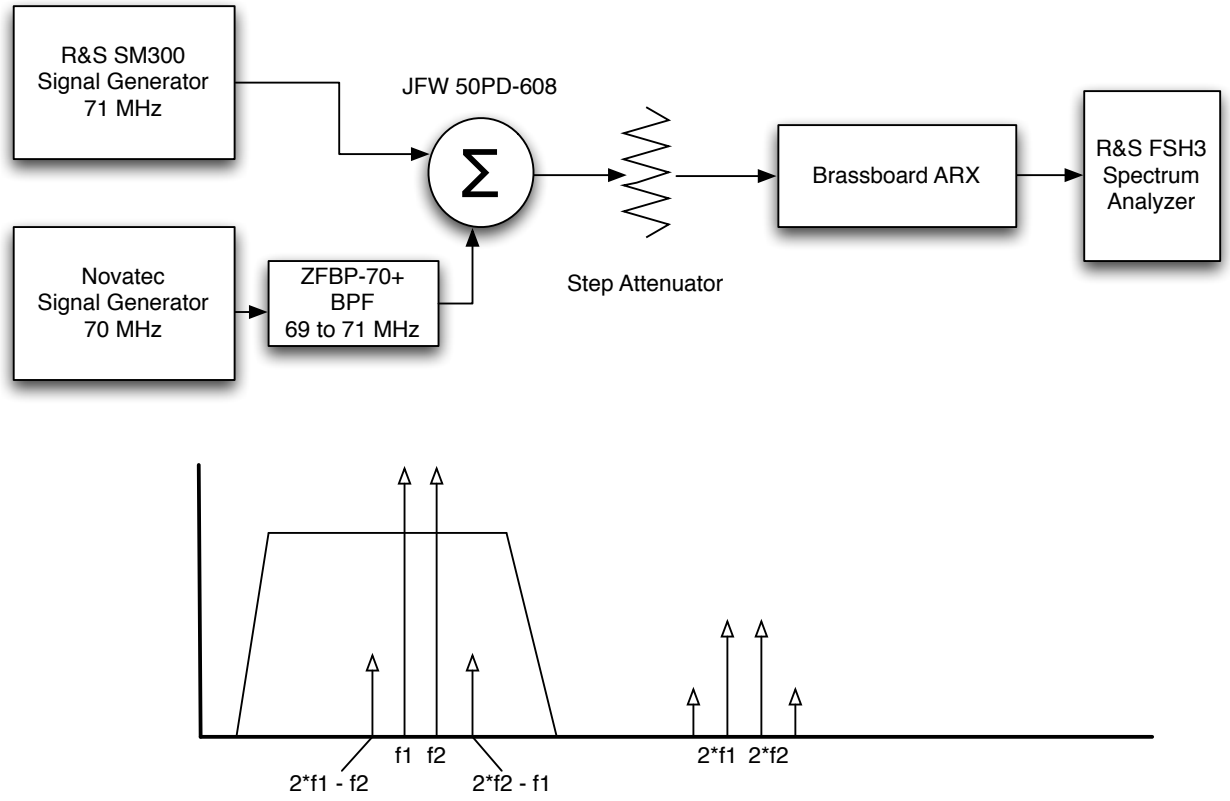


Figure 7: Two-Tone IIP3 Measurement Setup and Spectrum

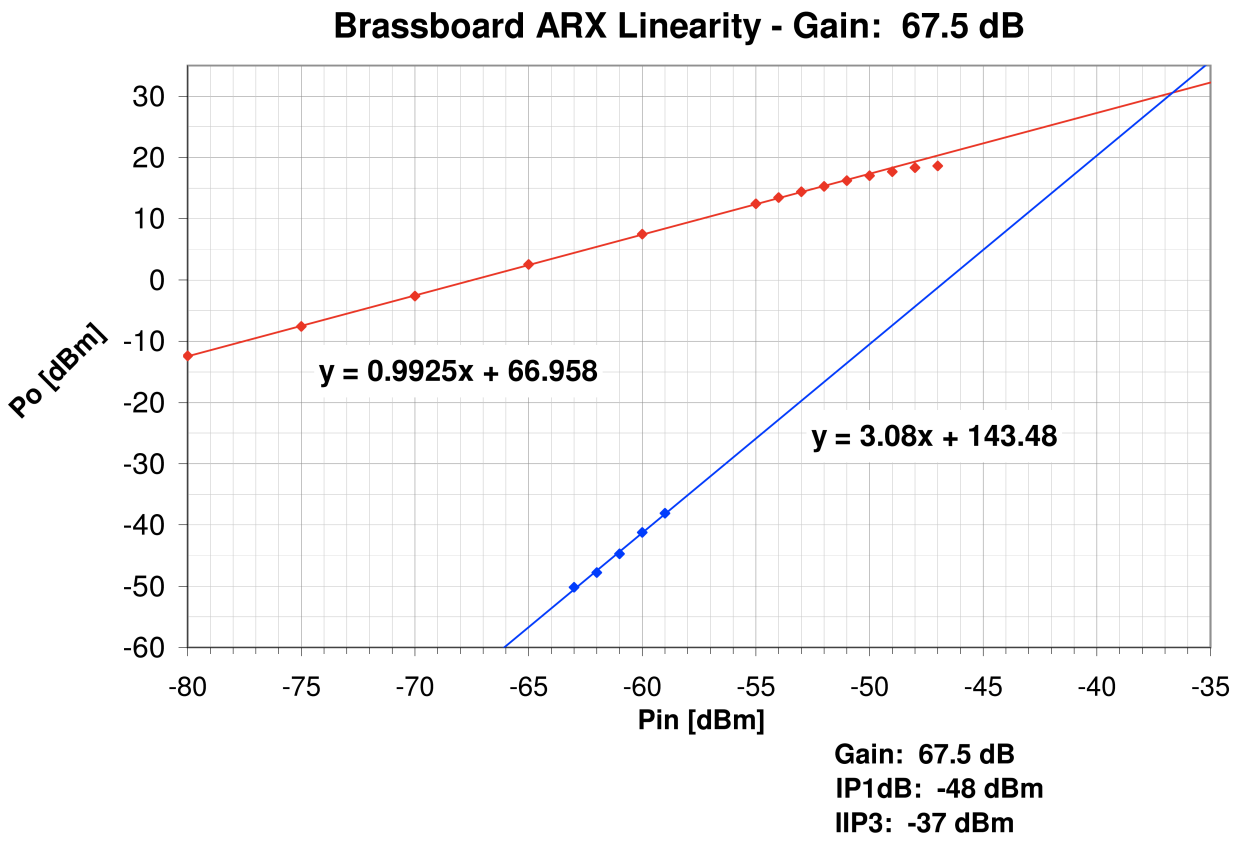


Figure 8: Gain and Linearity at 70 MHz

5. Channel-to-Channel Cross-Coupling

The coupling was measured with the receiver in full-bandwidth filter configuration, maximum gain setting. The RF shield (shown in Figure 9) was used in this test, but the same test should be performed with the shields removed. A signal was injected (38 MHz, -50 dBm) into one channel and measured at the output of the adjacent channel (diagramed in Figure 10). The cross-coupling is defined by (1).

$$C_{ch} = P_o - P_i - G \tag{1}$$

where,

P_o is the power out of ch.2
P_i is the power into ch.1
G is the channel gain

For a -50 dBm test-tone, the signal out of Ch.1 was measured at +18 dBm (Gain of +68dB), and the signal out of ch. 2 was measured at -46.5 dBm. The channel-to-channel cross-coupling is -64.5dB.

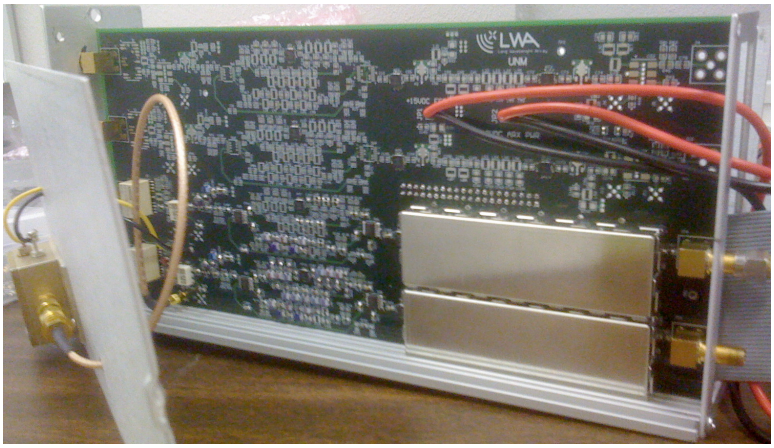


Figure 9: Brassboard ARX with RF shields isolating the final two gain stages

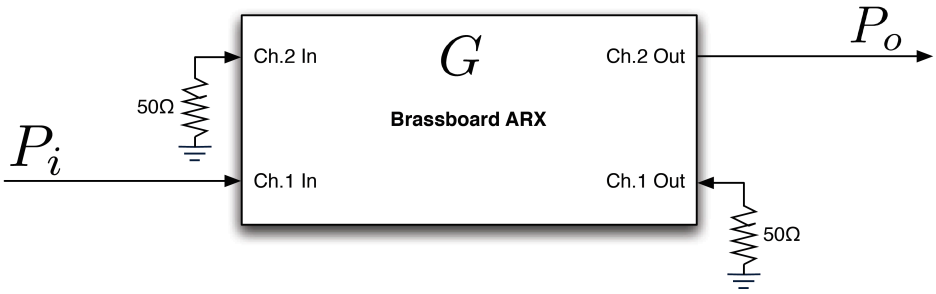


Figure 10: Channel-to-Channel Cross-Coupling Test Setup

References:

[1] Joe Craig, *ARX Requirements v1,* LWA Engineering Memo, June 16, 2008

Interface Control Document

Between: Analog Signal Processing MCS (ASP-MCS)
And: Station Monitor and Control (ST-MCS)

Status: Draft for PDR Release
2008-11-13

Prepared By	**Date**
J. Craig	2008-11-13
System Engineering Approval	**Date**
J. Craig	YYYY-MM-DD
System Architecture Approval	**Date**
L. Rickard	YYYY-MM-DD

Change Record

Version	Date	Affected Section(s)	Reason/Initiation/Remarks
A	2008-11-12	All	Initial Template Draft

Table of Contents

List of Tables

List of Figures

1 DESCRIPTION

1.1 Purpose

The purpose of this document is to define the Station Monitor and Control, Level-1 interface between the Analog Signal Processing Monitor and Control (ASP-MCS). The ASP described here is used to adjust the gains of each antenna signal, send power to the Front-End Electronics (FEE), and provide adequate filtering of the RF signal prior to digitization.

1.2 Scope

The document contains lists of monitor and control points available in the ASP and their suggested access rates.

1.3 Related Documents and Drawings

All EMs, LWA Memos, schematics, module drawings, wiring diagrams, other ICDs, etc.

1.4 Applicable Documents and Drawings

ICD definition document, station architecture, technical requirements, etc.

1.5 Order of precedence

In the event of conflict between the text of this document and applicable documents, the applicable documents shall take precedence unless explicitly mentioned in this document.

2 ABBREVIATIONS AND ACRONYMS

See [EM XXX]

2.1 Glossary

See [EM XXX]

3 PHYSICAL SYSTEM INTERFACES

3.1 Mechanical Interface

See [EM XXX]

3.2 Electrical Power Interface

See [EM XXX]

3.3 Electronic Interface

Describe the monitor/control electronics

3.3.1 List of Connectors

The connection between the MCS and the ASP will be an XXX cable in the receiver rack of the electronics shelter.

4 SOFTWARE/CONTROL FUNCTION INTERFACE

4.1 Overview

The ASP-MCS module consists of a single software controllable component.

4.1.1 MCS Interface

Describe the MCS Interface.

4.1.2 Filter Configuration

Describe the ARX Filter Configuration settings.

4.1.2 Gain Control

Describe the ARX Gain Control settings.

4.1.2 FEE Power

Describe the FEE Power settings.

4.2 Software/Control Function

See Sections 4.4 and 4.5.

4.3 Monitor & Control Functions

See Sections 4.4 and 4.5.

4.4 Summary of Monitor Points

Monitor data shall be polled by the MCS system according to the protocol specified in [EM XXX].

Table 1: Summary of Monitor Points

Name	Addressing	Data Size (bytes)	Suggested Interval (secs)	Timing Event Related?
GET_FILTER	XXXX	1	XXXX	No
GET_ATTN_1	XXXX	1	XXXX	No
GET_ATTN_2	XXXX	1	XXXX	No
GET_SPLIT_ATTN	XXXX	1	XXXX	No
GET_FEE_PWR	XXXX	1	XXXX	No
GET_TEMP	XXXX	XXXX	XXXX	No
GET_MODULE_CODE	XXXX	XXXX	XXXX	No

4.5 Summary of Control Points

Control data shall be transmitted by the MCS system according to the protocol specified in [EM XXX].

Table 2: Summary of Control Points

Name	Addressing	Data Size (bytes)	Suggested Interval (secs)	Timing Event Related?
SET_FILTER	XXXX	1	XXXX	No
SET_ATTN_1	XXXX	1	XXXX	No
SET_ATTN_2	XXXX	1	XXXX	No
SET_SPLIT_ATTN	XXXX	1	XXXX	No
SET_FEE_PWR	XXXX	1	XXXX	No
SET_MODULE_CODE	XXXX	XXXX	XXXX	No
RESET	XXXX	XXXX	XXXX	No

4.6 Other Software

4.6.1 Monitor Points in Detail

4.6.1.1 GET_FILTER

Addressing	*XXXX*
Description	*This is a read back of the SET_FILTER command. It is used to verify that the ARX has received the previous SET_FILTER command. It will return "Full Bandwidth" if the SET_FILTER command has never been called. The default filter upon power up of the ARX is "Full Bandwidth".*
Suggested Interval	*XXXX seconds*
TE Related	*No*
Data	*1 Byte: (uint8)*
Conversion Factor	*0x00 = Split Bandwidth Filter Configuration* *0x01 = Full Bandwidth Filter Configuration* *0x02 = Reduced Bandwidth Filter Configuration* *0x03 = Signal Chain OFF*
Operating Range	*N/A*

4.6.1.2 GET_ATTN_1

Addressing	*XXXX*
Description	*This is a read back of the SET_ATTN_1 command. It is used to verify that the ARX has received the previous SET_ATTN_1 command. It will return 30dB if the SET_ATTN_1 command has never been called. The default attenuator 1 setting upon power up of the ARX is 30dB.*
Suggested Interval	*XXXX seconds*
TE Related	*No*
Data	*1 Byte: (uint8)*
Conversion Factor	*0x00 to 0x0F = 0 dB to 30 dB* *LSB = 2 dB*
Operating Range	*0 dB to 30 dB, 2 dB steps*

4.6.1.3 GET_ATTN_2

Addressing	*XXXX*
Description	*This is a read back of the SET_ATTN_2 command. It is used to verify that the ARX has received the previous SET_ATTN_2 command. It will return 30dB if the SET_ATTN_1 command has never been called. The default attenuator 2 setting upon power up of the ARX is 30dB.*
Suggested Interval	*XXXX seconds*
TE Related	*No*
Data	*1 Byte: (uint8)*
Conversion Factor	*0x00 to 0x0F = 0 dB to 30 dB* *LSB = 2 dB*
Operating Range	*0 dB to 30 dB, 2 dB steps*

4.6.1.4 GET_SPLIT_ATTN

Addressing	*XXXX*
Description	*This is a read back of the SET_SPLIT_ATTN command. It is used to verify that the ARX has received the previous SET_SPLIT_ATTN command. It will return 30dB if the SET_SPLIT_ATTN command has never been called. The default split bandwidth attenuator setting upon power up of the ARX is 30dB.*
Suggested Interval	*XXXX seconds*
TE Related	*No*
Data	*1 Byte: (uint8)*
Conversion Factor	*0x00 to 0x0F = 0 dB to 30 dB* *LSB = 2 dB*
Operating Range	*0 dB to 30 dB, 2 dB steps*

4.6.1.5 GET_FEE_PWR

Addressing	*XXXX*
Description	*This is a read back of the SET_FEE_PWR command. It is used to verify that the ARX has received the previous SET_FEE_PWR command. It will return All Off if the SET_FEE_PWR command has never been called. The default FEE Power setting upon power up of the ARX is All Off.*
Suggested Interval	*XXXX seconds*
TE Related	*No*
Data	*1 Byte: (uint8)*
Conversion Factor	*0x00 = All Off* *Bit 0 = Channel 1* *Bit 1 = Channel 2* *Bit 2 = Channel 3* *Bit 3 = Channel 4* *Logic High = Channel ON* *Logic Low = Channel OFF*
Operating Range	*Channel 1 to Channel 4*

4.6.1.6 GET_TEMP

Addressing	*XXXX*
Description	*This is a read back of the ARX temperature monitor points. Currently NOT implemented.*
Suggested Interval	*XXXX seconds*
TE Related	*No*
Data	*XXXX*
Conversion Factor	*XXXX*
Operating Range	*XXXX*

4.6.1.7 GET_MODULE_CODE

Addressing	*XXXX*
Description	*This is a read back of the ARX module identification code. Currently NOT implemented.*
Suggested Interval	*XXXX seconds*
TE Related	*No*
Data	*XXXX*
Conversion Factor	*XXXX*
Operating Range	*XXXX*

4.6.2 Control Points in Detail

4.6.2.1 SET_FILTER

Addressing	*XXXX*
Description	*Sets the ARX Filter Configuration. This value can be set for one of the 4 possible filter configuration modes: Split Bandwidth, Full Bandwidth, Reduced Bandwidth, or Signal Chain OFF.*
Suggested Interval	*Initialization*
TE Related	*No*
Data	*1 Byte: (uint8)*
Conversion Factor	*0x00 = Split Bandwidth Filter Configuration* *0x01 = Full Bandwidth Filter Configuration* *0x02 = Reduced Bandwidth Filter Configuration* *0x03 = Signal Chain OFF*
Operating Range	*N/A*

4.6.2.1 SET_ATTN_1

Addressing	*XXXX*
Description	*Sets the value of ARX attenuator 1. This value can be set from 0 dB to 30 dB, in 2 dB steps.*
Suggested Interval	*Initialization*
TE Related	*No*
Data	*1 Byte: (uint8)*
Conversion Factor	*0x00 to 0x0F = 0 dB to 30 dB* *LSB = 2 dB*
Operating Range	*0 dB to 30 dB, 2 dB steps*

4.6.2.2 SET_ATTN_2

Addressing	*XXXX*
Description	*Sets the value of ARX attenuator 2. This value can be set from 0 dB to 30 dB, in 2 dB steps.*
Suggested Interval	*Initialization*
TE Related	*No*
Data	*1 Byte: (uint8)*
Conversion Factor	*0x00 to 0x0F = 0 dB to 30 dB* *LSB = 2 dB*
Operating Range	*0 dB to 30 dB, 2 dB steps*

4.6.2.3 SET_SPLIT_ATTN

Addressing	*XXXX*
Description	*Sets the value of split bandwidth attenuator. This value can be set from 0 dB to 30 dB, in 2 dB steps.*
Suggested Interval	*Initialization*
TE Related	*No*
Data	*1 Byte: (uint8)*
Conversion Factor	*0x00 to 0x0F = 0 dB to 30 dB* *LSB = 2 dB*
Operating Range	*0 dB to 30 dB, 2 dB steps*

4.6.2.4 SET_FEE_PWR

Addressing	*XXXX*
Description	*Sets the power to individual FEE channels ON or OFF.*
Suggested Interval	*Initialization*
TE Related	*No*
Data	*1 Byte: (uint8)*
Conversion Factor	*0x00 = All Off* *Bit 0 = Channel 1* *Bit 1 = Channel 2* *Bit 2 = Channel 3* *Bit 3 = Channel 4* *Logic High = Channel ON* *Logic Low = Channel OFF*
Operating Range	*Channel 1 to Channel 4*

4.6.2.5 SET_MODULE_CODE

Addressing	*XXXX*
Description	*Sets the ARX module identification code.* *Currently NOT implemented.*
Suggested Interval	*XXXX seconds*
TE Related	*No*
Data	*XXXX*
Conversion Factor	*XXXX*
Operating Range	*XXXX*

4.6.2.6 RESET

Addressing	*XXXX*
Description	*Issues a RESET to the ARX.* *Currently NOT implemented.*
Suggested Interval	*XXXX seconds*
TE Related	*No*
Data	*XXXX*
Conversion Factor	*XXXX*
Operating Range	*XXXX*

5 SAFETY INTERFACE

The ARX has no safety issues requiring frequency monitoring. No action of the monitor and control system can cause incorrect or dangerous conditions in the ARX.

ARX Split Bandwidth Filter Configuration
Joe Craig
11/14/08

Below are plots for the Split Bandwidth Filter Configuration after adding a 6 dB Pi-Pad attenuator between the two HPF sections. This seems to mediate the previous problem of resonance by isolating the filter sections.

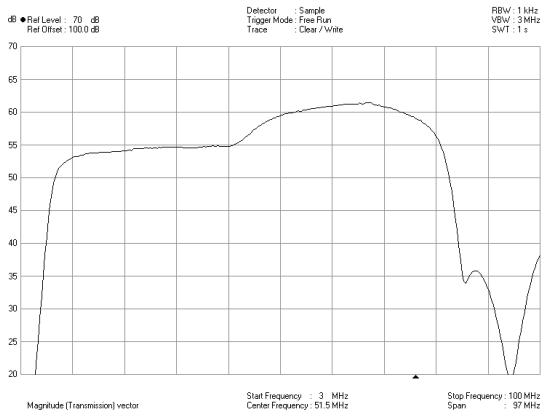


Figure 1: Split Bandwidth Filter Configuration - 6dB Down - S21 Magnitude

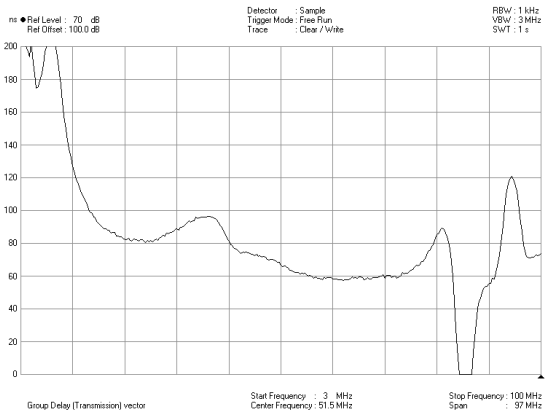


Figure 2: Split Bandwidth Filter Configuration - 6dB Down - S21 Group Delay

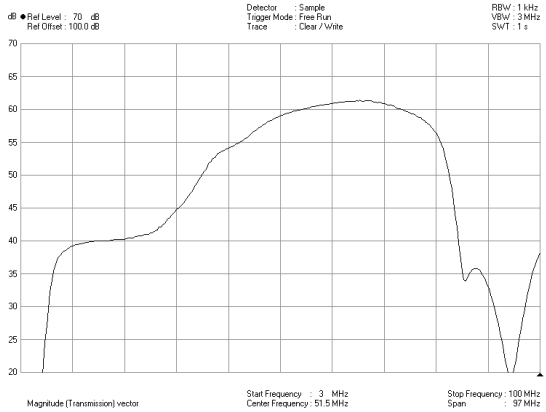


Figure 3: Split Bandwidth Filter Configuration - 20dB Down - S21 Magnitude

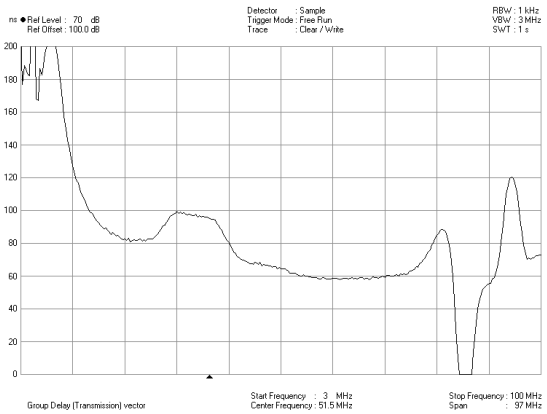


Figure 4: Split Bandwidth Filter Configuration - 20dB Down - S21 Group Delay

Preliminary Design of the LWA Analog Signal Processor

Joe Craig*

February 4, 2009

Contents

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1 Introduction

This document describes the preliminary design of the Long Wavelength Array (LWA) Analog Signal Processor (ASP). As detailed in LWA Memo 119 [1], the ASP contains:

- Analog Receiver (ARX): This is the antenna receivers which provide adequate gain and selectivity prior to digitization. There are 512 individual ARX receiver channels per station (256 antennas x 2 polarizations).
- Analog Array Processor (AAP): Placeholder subsystem for analog beamforming (as necessary).
- Power Conditioning & Distribution (ASP-PCD): Power for Receivers and Front-End Electronics (FEE).
- Monitoring & Control System (ASP-MCS): ASP Monitor/Control to Station MCS.
- Electromechanical Design (ASP-EMD): Receiver packaging and ASP electronics physical rack layout.

The preliminary design for each Level-2 subsystem above, is given in section 2.

2 Level-2 Subsystem Design

The ASP for a single station will be housed in one standard 19" electronic equipment rack. The 512 analog signals pass from the Shelter Entry Panel (SEP) [5] to the ARXs via coaxial cable and bulkheads at the ASP rack. The ARX controls the gain and selectivity (filtering) of the analog signals from each dipole element before transporting the signal (differentially) to the Digitizer (DIG) subsystem in the Digital Processor (DP).

The ASP is also responsible for delivering power to the FEEs at each antenna via a bias-tee (integrated into the ARXs). The ASP Power Conditioning and Distribution (ASP-PCD) converts the station AC power to DC power for the FEEs and ARXs. The ASP is a single node on the station MCS network and communicates the monitor points and configuration commands to the ARXs and ASP-PCD via a gigibit ethernet connection to the station MCS.

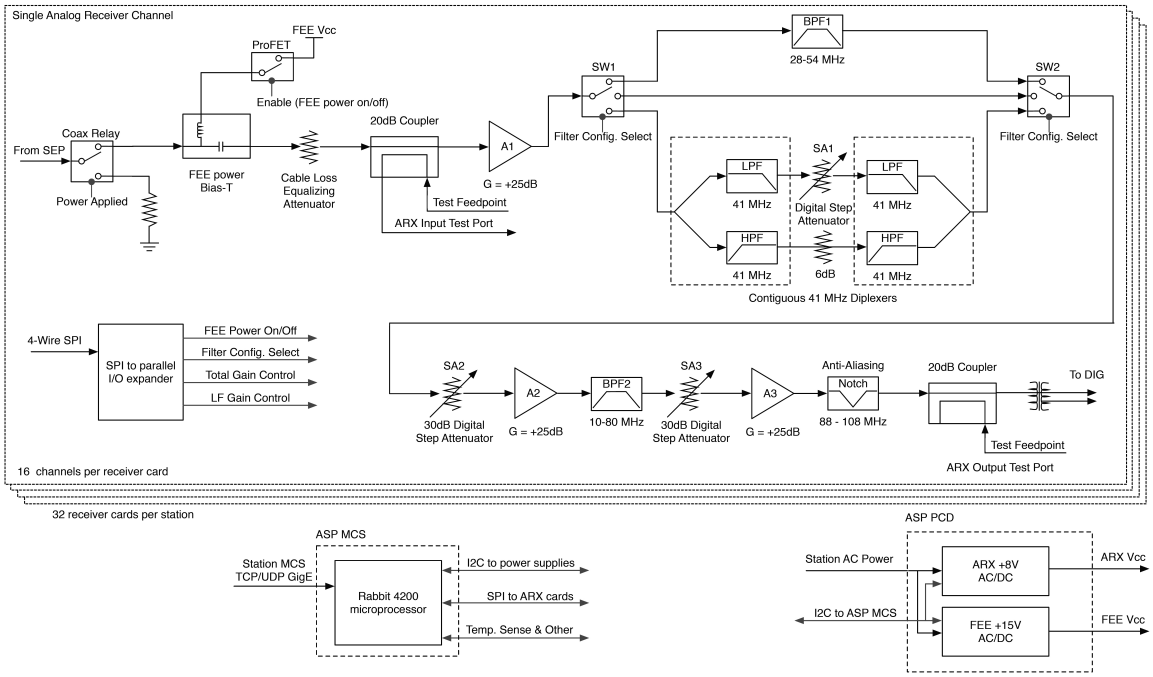


Figure 1: ASP Block Diagram, detailing the electronics of the ARX.

2.1 Analog Receiver (ARX)

LWA Memo 121 [2] derives general requirements for the LWA analog receivers. A full set of ARX requirements is given in [8]. A summary of the ARX requirements (assuming LWA Memo 120 [3] FEE is used) is shown in Table 1. These requirements have been derived to provide adequate gain (and control) of the signal before reaching the digitizer, maintaining a total noise figure comparable to that of the FEE (2.7 dB) and providing appropriate system linearity in the presence of RFI levels measured at potential LWA site.

Table 1: ARX Gain, Noise Figure, and Linearity Requirements

Receiver Configuration	G [dB]	F [dB]	IP1dB [dBm]	IIP3 [dBm]
ARX Max Gain	65	7	-62	-47
ARX Min Gain	5	11	-17	-2

A set of ARX features are discussed in [2], [8], [9], and [10]. These features are summarize below.

- *Reconfigurable Filter Bank:* The ARX incorporates a reconfigurable filter bank, allowing selection of three filter configurations:
  - *Full Bandwidth Filter:* 3 dB Passband of 10 MHz to 88 MHz.
  - *Reduced Bandwidth Filter:* 3 dB Passband of 28 MHz to 54 MHz.
  - *Split Bandwidth Filter:* 3 dB Passband of 10 MHz to 88 MHz, with additional attenuation control over the low frequency portion of the passband (diplexed at 41 MHz).
- *Gain Control:* The ARX provides 60 dB of gain control via two digital step attenuators operating in 2 dB steps. The two attenuators are placed in the receive chain in such a way that the system linearity and noise figure can be prioritized. For instance, the system achieves better linearity at the cost of noise figure by setting the first attenuator at a higher value than the second attenuator.
- *Bias-Tee for FEE Power:* Each ARX channel provides a bias-tee circuit for distributing power to the FEEs. A TTL logic compatable switch is incorporate for power on/off to the FEEs through the ARX.
- *Signal Test Ports:* Each ARX channel provides a coupled port for either injecting signals or analyzing signals at both ARX inputs and outputs.
- *Independent Channel Control:* The ARX provides the ability to address any single dipole receiver and configure the filters and gains independently of other the other channels.
- *Input Protection:* The ARX provides a coaxial relay to physically isolate the inputs from the rest of receive chain when not in use. This is an extra level of security against lightning and ESD.

A prototype ARX (aka Brassboard ARX) has been developed by UNM (Figure 2) and is described in [9], [10], and [11]. Its measured characteristics are detailed in [11]. The Brassboard ARX provides 68 dB of gain, with 60 dB of gain control in 2 dB steps, a reconfigurable filter bank with three filter configurations (summarized above), and an integrated bias-tee for powering the FEEs. The Brassboard ARX meets (or exceeds) the requirements of Table 1. An image of the circuit board layout is provided in Figure 3. The magnitude response of the ARX in maximum gain configuration is shown in Figure 4. *In Situ* evaluation of the Brassboard ARX was conducted at the LWDA site (located at the VLA in NM). A prototype antenna [12], 150 m of cable, and prototype digitizer/data capture [4] was used in this evaluation. The resulting data for all three filter configurations is shown in Figure 6. The same signal path (replacing the antenna with a load resistor) was evaluated in the lab. The results are shown in Figure 5 and demonstrates galactic noise dominance above the noise temperature of the receiver.

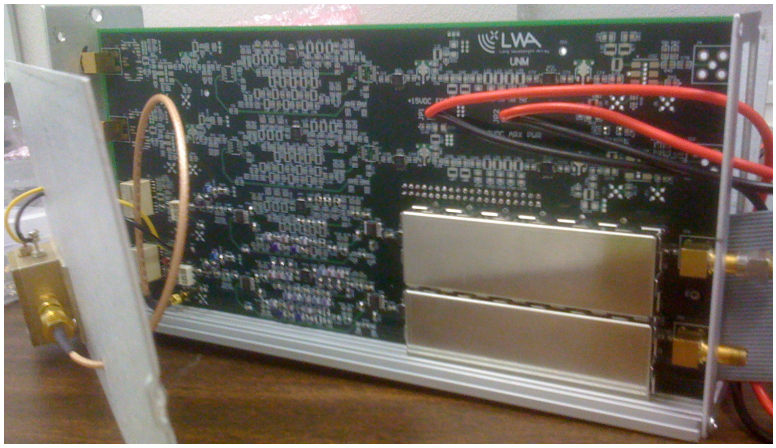


Figure 2: Brassboard ARX Module developed at UNM.

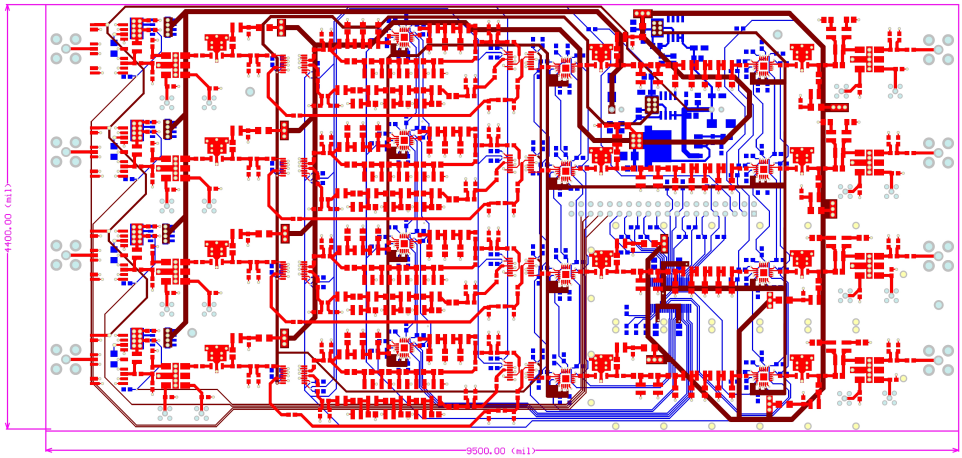


Figure 3: ARX Brassboard circuit board layout.

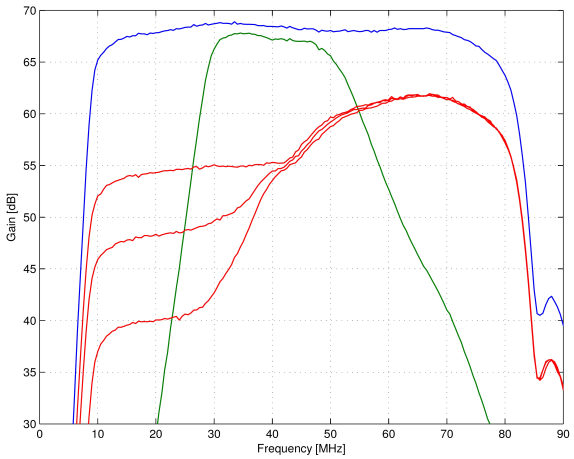


Figure 4: ARX Brassboard Magnitude Response in Full Gain configuration. The blue curve is the Full Bandwidth filter, the green curve is Reduced Bandwidth, and the Red curve is Split Bandwidth (shown for 6 dB, 12 dB, and 20 dB down).

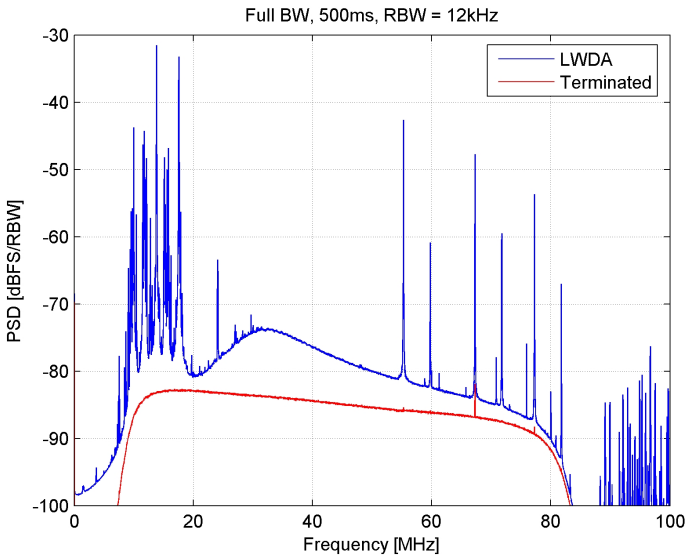


Figure 5: ARX Brassboard terminated in the lab (receiver noise floor) with sky data overlayed. This demonstrates the receiver is galactic noise dominated.

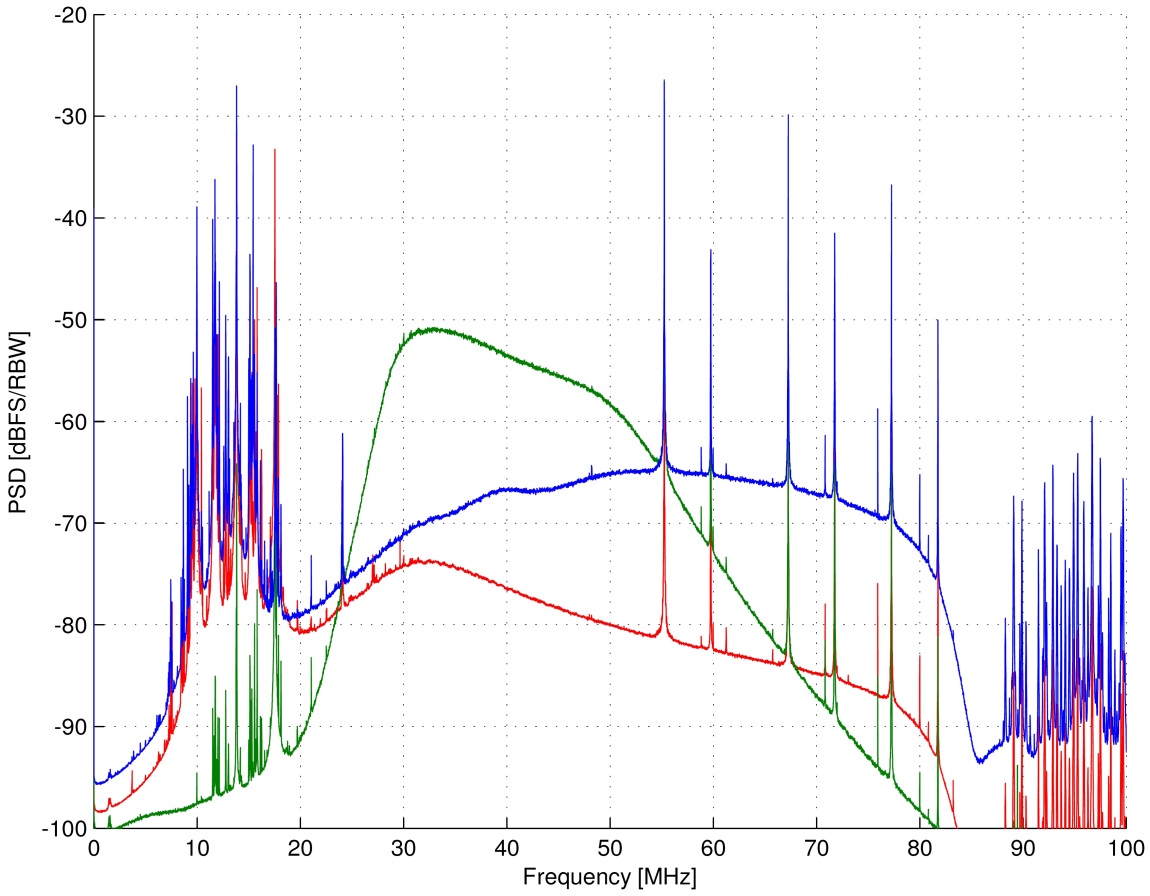


Figure 6: ARX Brassboard *in situ* evaluation. The ARX gains were adjusted according to the current RFI conditions for a maximum RFI peak around -10 dBFS/RBW (full-scale digitizer dynamic range is 0 dBFS/RBW). The red curve shows the Full Bandwidth filter, the green curve is the Reduced Bandwidth filter, and the blue curve is the Split Bandwidth filter set to 12 dB down. The spectral data has been integrated for about 200 msec. RBW is 12 kHz. No attempt has been made to calibrate the data against cable loss or antenna impedance.

2.2 Analog Array Processor (AAP)

The AAP was originally defined to identify the possiblity that analog beamforming would be required. Since the preliminary design of the Digital Processor (DP) provides the functionality of full-bandwidth beamforming, the AAP subsystem is no longer required for beamforming. Instead, the AAP should be considered a subsystem that could provide useful analog signal diagnostics and/or test hardware as required for commissioning and troubleshooting. The ARX (section 2.1) provides signal access for both the input of ARX (signal from each dipole) and the output of ARX (after gain and filtering). The AAP may consist of an RF switch matrix, signal generator and/or spectrum analyzer for analog signal path verification and troubleshooting. Injecting signals at the ARX may prove to be valuable in verifying and diagnosing the entire processing chain on an invidual dipole level, including the DP subsystem.

2.3 Monitoring and Control System (ASP-MCS)

The ASP-MCS consists of a microcontroller which translates ethernet packets to various other digital interfaces. There is very little data passing along this interface as it used primarily for setting gains and filter configurations in the ARXs. Power supply status information can also be obtained through the ASP-MCS interface.

The RabbitCore RCM4200 development board [6] provides all the functionality required of the ASP-MCS. The Rabbit board features a microprocessor running at 60 MHz, with 8 Mbytes of serial flash memory, an SPI interface for communication with ARXs, an I^2C port for power supply communications, and and an A/D converter which can be used for temperature monitoring.

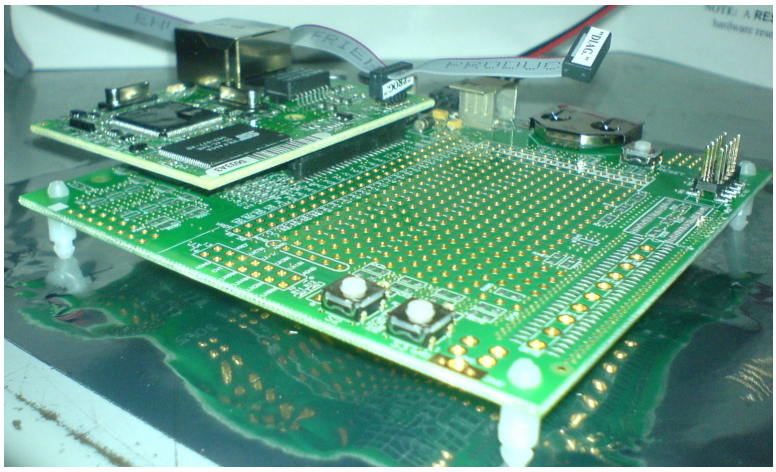
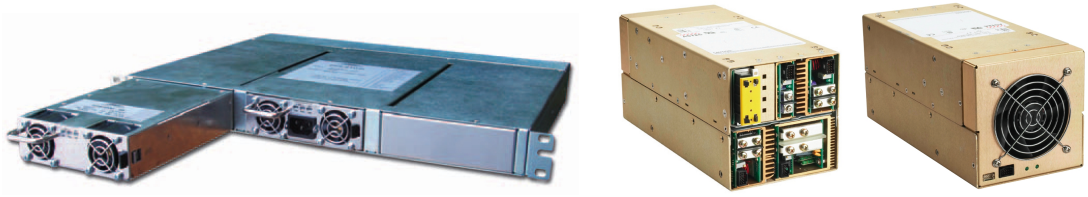


Figure 7: The heart of the ASP-MCS, the RabbitCore RCM4200 development board.

2.4 Power Conditioning and Distribution (ASP-PCD)

The ASP provides power to the ARXs and to the FEEs at the antenna from a clean AC voltage distributed by the Station Power Conditioning and Distribution (SHL-PCD). There is no need for backup power (UPS) at the ASP since there are no computers that need to shut down in case of power outages. It is also useful to have remote access to the ASP-PCD through the Station MCS. The ASP-MCS will provide a communication interface (most likely I^2C) to remote shutdown/cycle power and monitor the output current.

The Brassboard ARX was designed to accept an input of +8 VDC at a steady current draw of approximately 250 mA per channel. For the 512 channels needed at a station, the ASP ARX power supplies must be capable of deliverying at least 1.1 kW. The prototype FEE accepts an input of +15.5 VDC at a steady current draw of approximately 230 mA per dipole [7]. For the 512 FEE dipoles at a station, the ASP FEE power supplies must be capable of delivering at least 1.8 kW. The supplies will likely be multiple COTS modules, wired in parallel. Candidate power supplies are shown in Figure 8.



(a) TDK-Lambda FPS series

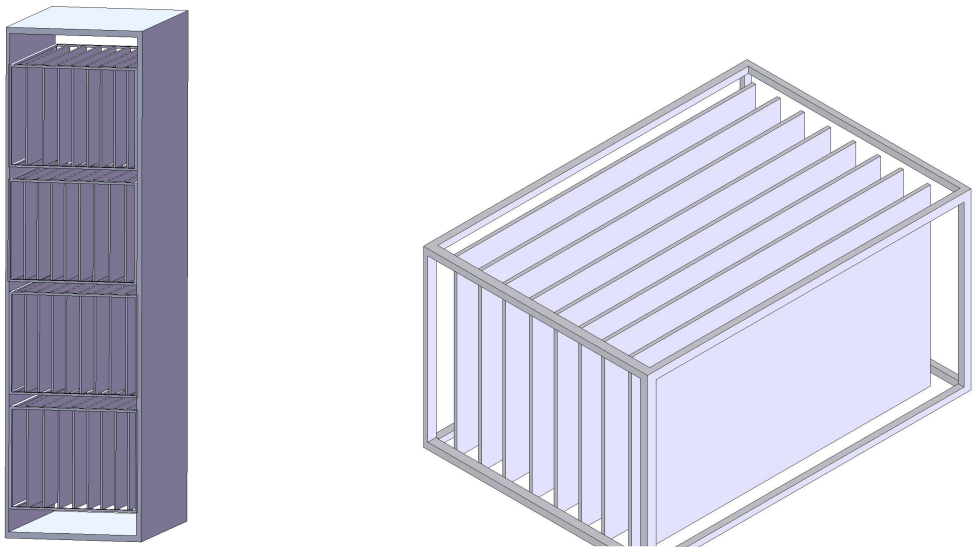
(b) Emerson-Astec iVS series

Figure 8: Two candidate ASP power supplies being considered.

2.5 Electromechanical Design (ASP-EMD)

The electromechanical design of the ASP provides a significant challenge since so many receiver channels are required per station. The problem of interconnects is greatly reduced if all the ARXs can fit in a single rack. Air/heat flow considerations become complex when the receiver packaging is the traditional "module" form. It is much simpler (and less expensive) to package the receiver cards in an open-frame chassis. RFI considerations can be minimized by providing metalized "cans" or "shields" on each receiver channel.

The ARX Brassboard demonstrates the ability to space receiver channels every 1.125". Standard Printed Circuit Board (PCB) panels can accomodate board areas up to 16" x 22". This means that 16 channels could easily fit on one PCB panel. Imagine each ARX chassis, illustrated in Figure 6(b), holds 8 receiver card (16 channels each). 4 of these ARX chassis would be required to provide 512 channels needed at a station, see Figure 6(a). The number of channels per circuit board may be reduced to provide modularity in the ARX design. The preliminary ASP-EMD design demonstrates the ability to house the entire 512 ARX receivers in one 19" equipment rack. The ASP-PCD and ASP-MCS may fit in this rack also, but an extra half rack should be allocated just in case.



(a) Conceptual design of ARXs in the ASP rack.

(b) Conceptual design of an ARX chassis.

Figure 9: Dimensional modeling of the Analog Signal Processor.

3 ASP Internal Interfaces

This section defines the internal interface connections specifically for the ASP (level-2) subsystems. The level-1 ASP interfaces are defined in [**?**].

- *Rack to ARX signal interface*
  The 512 signal cables enter the electronics shelter at the Shelter Entry Panel (SEP), terminated with N-type bulkhead connectors. The signals are then passed to the ASP rack via coaxial cable. The ASP rack will have an entry panel (likely on the side) for all 512 signals. The type of connector will be a standard RF coaxial termination (N-type, SMA, BNC, etc.), and will be chosen primarily on ease of installation/maintance and EMI leakage characteristics.

- *ARX to Rack signal interface*
  The individual ARX card signal input will likely be a ganged (high-density) RF cable, such that only one signal connection to each card is required. A signal distribution board may be designed from the rack bulkhead connections to the ARX card input, or an appropriate cable assembly will be used. One idea is to design a distribution board at the chassis level, which connects to each ARX card via board-to-board RF connector (similar to a backplane), and route the signals to a cable assembly for connection to the bulkheads.

- *PCD to ARX interface*
  The power to ARX cards will be distributed via two separate lines (ARX power and FEE power). In the event that a distribution board is designed for RF signals, the power distribution to each receiver card may be incorporated onto the same board.

- *MCS to ARX interface*
  Since each ARX channel requires XX number of parallel logic bits for control, distributing the logic in parallel (as used in the Brassboard ARX) is not an option. Instead, the logic will be distributed to each receiver card via a serial interface. The specific protocol has not yet been selected, but investigation into 4-wire SPI is currently underway. A daisy-chain architecture is the most reasonable for this design since SPI devices exist that are individually addressable.

- *MCS to PCD interface*
  The power supplies being considered allow remote access and control to functions such as power on/off and output current information. The current protocols being considered are I^2C, SPI, and RS-232.

4 Manufacturing, Qualification and Installation

The ARX electronics will be built by a turnkey circuit board fab. house. The fab. house will provide the essential functional board level tests. Certain parts may be provided to this fab. house due price breaks available through the LWA/UNM project office. Once the ASP design passes the Critical Design Review (CDR), it is estimated that the full ARX build for ASP will be less than 3 months. The mechanical design of the ARX chassis will likely be fabricated by a local machine shop and is estimated to be less than 2 months, once the design passes at the CDR level. Qualification testing of the receivers will be done in-house (at UNM). Assembly and installation of the ASP will occur in two sequential steps:

- *In-House Assembly and Qualification*
  The entire ASP rack will be assembled at UNM and pass fit/form/functional testing. All receiver channels will be exercised within their final configurations (through MCS, using PCD).

- *Field Installation*
  Upon successful qualification in-house, the ASP will be transported to the LWA1 site for installation and system integration. Whether the rack is delivered to the site fully-integrated, or the ASP integration happens at the site is currently TBD.

The ASP assumes certain subsystems are in place before system integration. The Level-1 subsystems that must be installed prior to ASP are RPD, SHL, and PCD. It would be beneficial for ASP installation and integration to occur after STD has been installed, but not absolutely necessary.

5 Cost Estimate

The ASP pile-of-parts cost estimate for LWA-1 is given in Table 2. The cost estimate for the ARX has been generated using information gathered in the design of the Brassboard ARX. These numbers are rough estimates and are provided for project budgetary purposes.

Table 2: ASP Parts Cost Estimate

Component	Cost per Channel (dipole)	LWA1 Parts Cost for ASP
SEP to ARX Cabling & bulkheads	$40-$50	$25k
ASP Power Supplies	-	$5k
Modified RFI Shielded Rack	-	$10k
ARX Chassis	-	$5k
ASP-MCS	-	$1k
ARX Turnkey Electronics	$50	$26k
ASP to DP Cabling & bulkheads	$10-$20	$10k
Total	-	**$82k**

6 Acknowledgments

Many people have helped in the design of the Brassboard ARX and aided in the preliminary design of the ASP. These include S. Ellingson (VT), B. Hicks (NRL), P. Ray (NRL), R. Scott (NRAO), K. Morris (NRAO), and S. Ashton (NRAO).

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SPI Communication for ARX Channels - ARX0023

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March 18, 2009

Contents

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1 Background

The LWA Analog Receiver has 520 identical signal "channels" for processing the RF signal prior to digitization. Each channel has 3 step attenuators (5 bit), a filterbank RF switch (2 bit), and a Front End (FEE) power on/off control (1 bit). This is a total of 18 logic bits for each channel.

The conceptual ARX design had each channel being configured exactly the same as every other channel (gain and filter setting), thus only requiring one set of parallel I/O to control the entire 520 ARX channels. It has become evident that individual control of each channel would be desireable (cable length gain equalization, etc.). Obviously, controlling each channel independently with parallel I/O is not an option (this would require $520 \cdot 18 = 9360$ bits).

A daisy-chain architecture using the Serial Peripheral Interface (SPI) protocol has been tested minimally and proves to be a viable option for controlling each ARX channel independently. Since the two polarizations from each antenna stand will have exactly the same cable length, the number of SPI devices can be minimized by controlling both polarizations with the same SPI device (no independent control over polarizations). 260 SPI devices, chained together on a 4-wire SPI bus, provides a relatively simple way to achieve independent antenna stand control in the ARX.

This document outlines the prototype validation of the proposed ARX SPI bus control.

2 MAX7301 & SPI Daisy-Chain

The MAX7301 is a serial-interface I/O expander (or general-purpose I/ (GPIO) peripheral), and provides microprocessors with up to 20 to 28 ports [1]. The MAX7301 operates by writing 16 bits of data (1 command byte, 1 data byte) to the 4-wire SPI inputs. GPIO can be configured for input or output and controlled with registers read or written to via the SPI bus.

The SPI protocol requires 4 bits for operation. The specific ARX implementation is listed below:

- Master Out Slave In (MOSI) - Data line out of the ASP-MCS. DIN of ARX boards.
- Master In Slave Out (MISO) - Date line in to the ASP-MCS. DOUT of ARX boards.
- SPI Clock (SCLK) - The clock signal out of the ASP-MCS. SCLK of ARX boards.
- Chip Select ($\overline{CS}$) - Data line for initiating data read/write. SCS of ARX boards.

Each dual-polarization, stand receiver channel in the ARX needs one MAX7301 to provide all 18 bits of control. In order for each device to be addressable on the SPI bus, all MAX7301's must be daisy chained together, as shown in figure 1.

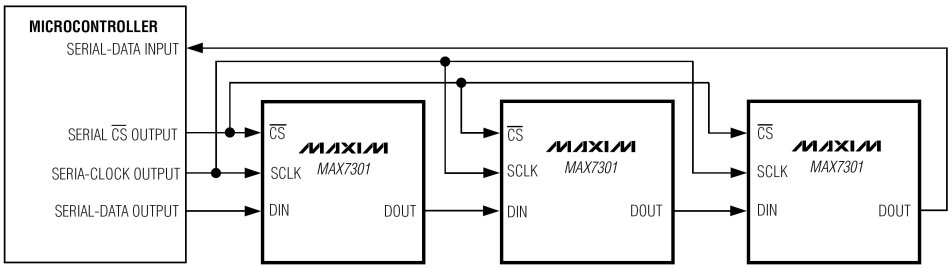


Figure 1: Daisy-chain architecture. The ARX daisy-chain will have 260 devices.

In order to address single devices, the No-Op command (0x00) must be sent to every other device on the chain. The ASP SPI bus could contain up to 260 individually addressable devices, so up to 260 commands could be initiated to change a single stand's bit settings. Data at the device's input port shows up 15.5 clock cycles later on the data ouput port. This allows the devices to pass data along the bus from one device to another. To change a setting on stand 260, that stand's control data would be sent first, then 259 No-Op commands to all the other devices. Alternatively, if a setting on stand 1 was desired, only one 16 bit command cycle would be necessary. This concept is illustrated in figure 2.

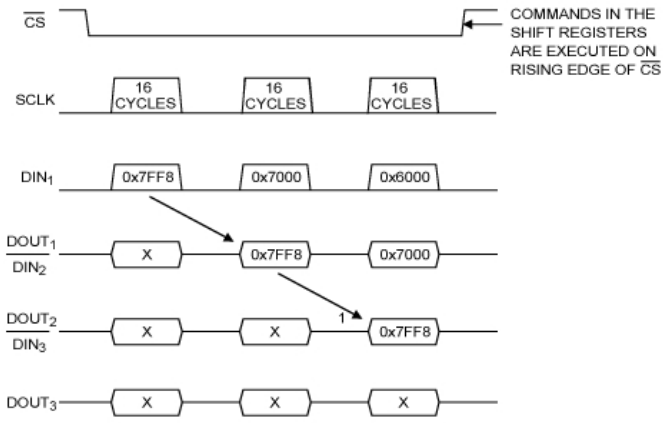


Figure 2: Typical daisy-chain command sequence.

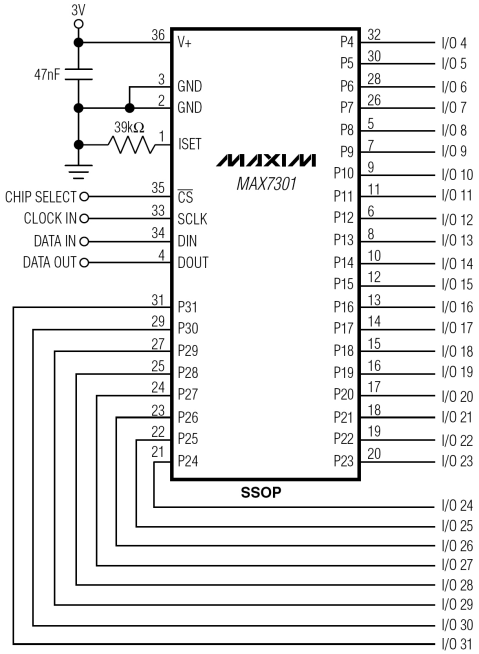


Figure 3: MAX7301 typical operating circuit.

3 Functional Test and Design Verification

Two MAX7301 devices have been daisy-chained together and controlled with the ASP-MCS Rabbit board. LEDs were connected to each board to indicate single bit control. Dynamic C code (Rabbit processor compiler language) was written to address each device indepedently and control the LEDs separately. Figure 4 shows one of the MAX7301 protoboards connected to the MCS Rabbit board. The code is provided in the appendix.

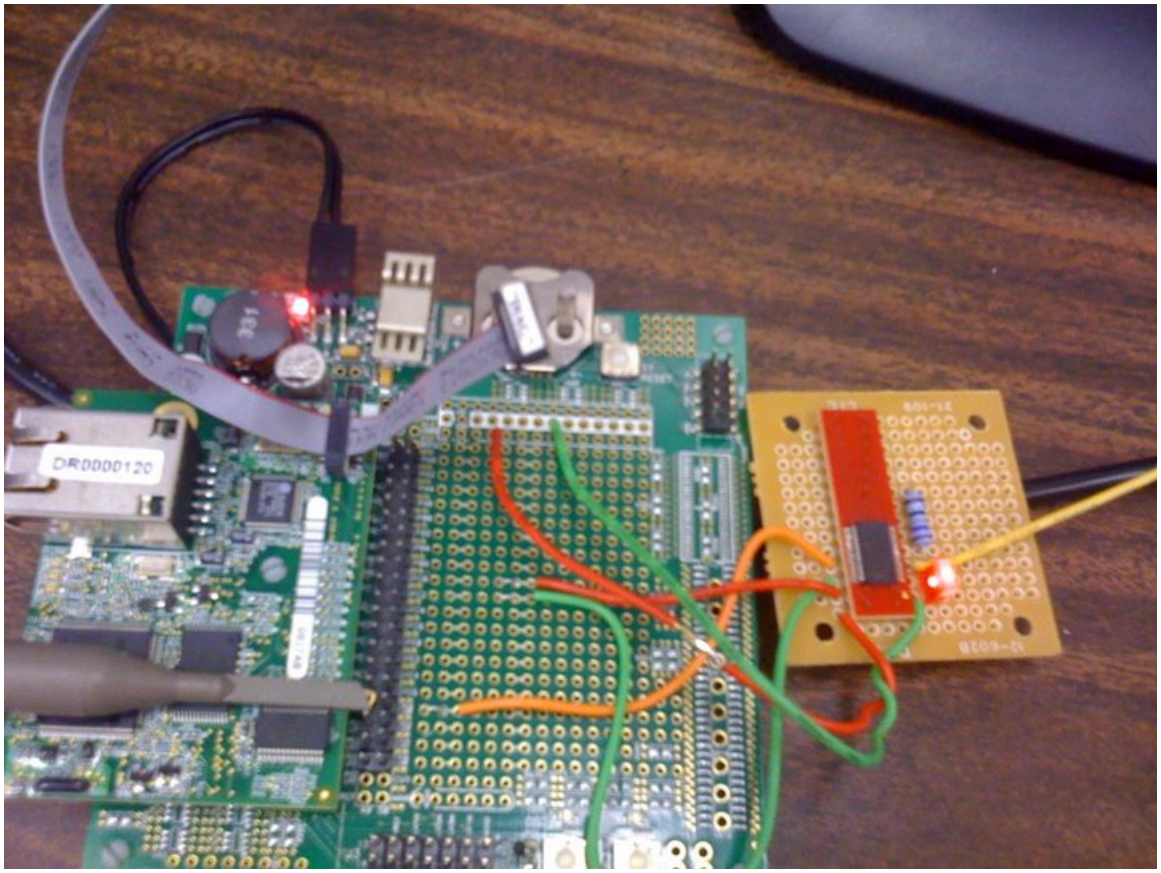


Figure 4: The Rabbit 4200 board and a single MAX7301 device flashing an LED.

References

[1] Datasheet, "4-Wire-Interfaced, 2.5V to 5.5V, 20-Port and 28-Port I/O Expander", MAX7301, April, 2006. http://www.maxim-ic.com.

4 Appendix - Dynamic C Code

```
/*****************************************
SPI routine test

SCLK on PE7
DOUT (MOSI) on PC2
DIN (MISO) on PE3
CS on PB7

*****************************************/

#define SPI_SER_C
#define SPI_RX_PORT SPI_RX_PE
#define SPI_CLK_DIVISOR 100

#use "spi.lib"
#use rcm42xx.lib

void SPI_init_devices(int num, int Config){
   int i, SPI_read;

   BitWrPortI(PBDR, &PBDRShadow, 0, 7);                    // chip select low
   for (i = 0; i < num; i++){
      SPIWrRd(&Config, &SPI_read, num);                  // setup for normal o
   }
   BitWrPortI(PBDR, &PBDRShadow, 1, 7);                    // chip select hig
}

void SPI_Send(unsigned data, int device, int num){
   int SPI_read, SPI_NoOp, i;
   SPI_NoOp = 0x0000;

   BitWrPortI(PBDR, &PBDRShadow, 0, 7);            // chip select low
   //printf("device is %02X\n", device);
   for (i = num; i > 0; i--){
      if (i == device){
         SPIWrRd(&data, &SPI_read, 2);             // write & read SPI
         //printf("sent: %04X\n", data);
      }
      else{
         SPIWrRd(&SPI_NoOp, &SPI_read, 2);              // write & read SPI
         //printf("sent: %04X\n", SPI_NoOp);
      }
   }
   BitWrPortI(PBDR, &PBDRShadow, 1, 7);            // chip select high
}

void main()
{
   int SPI_cfg_normal, SPI_cfg_output_P16_17_18_19, SPI_P16_on, SPI_P16_off;
   int SPI_read, num, i;

   num = 2;
   SPI_cfg_normal = 0x0104;
   SPI_cfg_output_P16_17_18_19 = 0x550C;
   SPI_P16_on = 0x0130;
   SPI_P16_off = 0x0030;

   brdInit();

   WrPortI(PCFR,&PCFRShadow,PCFRShadow | 0x44);       // Serial Port C
```

```
   WrPortI(PEAHR,&PEAHRShadow,PEAHRShadow | 0xC0);     // Serial Port C
   WrPortI(PEDDR,&PEDDRShadow,PEDDRShadow | 0x80);     // Serial Port C clock o
   WrPortI(PEFR,&PEFRShadow,PEFRShadow | 0x80);        // Serial Port C

   SPIinit();

   SPI_init_devices(num, SPI_cfg_normal);              //out of sleep mode
   SPI_init_devices(num, SPI_cfg_output_P16_17_18_19);   //set outputs


   while(1)
   {
      costate
      {
            SPI_Send(SPI_P16_on, 1, num);
            waitfor(DelayMs(50));

            SPI_Send(SPI_P16_on, 2, num);
            waitfor(DelayMs(50));

            SPI_Send(SPI_P16_off, 2, num);
            waitfor(DelayMs(50));

            SPI_Send(SPI_P16_on, 2, num);
            waitfor(DelayMs(50));

            SPI_Send(SPI_P16_off, 2, num);
            waitfor(DelayMs(50));

            SPI_Send(SPI_P16_off, 1, num);
            waitfor(DelayMs(50));
      }
   }
}
```

Trace Width Calculation for Analog Receiver Board
7/1/09
Joe Craig

Since the LWA Analog Receiver (ARX) boards require a significant trace length, it is important to find the optimal trace width to match the characteristic impedance of the transmission line. The input to the ARX circuit is 50 Ω, single-ended. The output from the ARX is 100 Ω differential. Both cases are modeled in ADS and tuned for matching. The optimal trace width for the microstrip on the ARX boards is 16 mils in the frequency range of 1 MHz to 100 MHz.

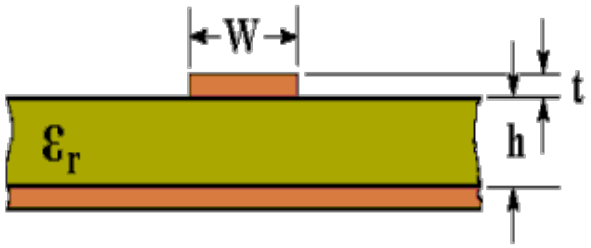


Figure 1: Microstrip circuit board stackup

Metrics used for calculating microstrip characteristic impedance, assuming a board thickness of 0.062", 4 layer (figure 2).

εr = 4.2 (FR4 relative dielectric constant)
W = !solve! (width of trace)
t = 1.4 mils (1 oz. copper trace thickness)
h = 8.9 mils (thickness of dielectric between ground plane and trace)

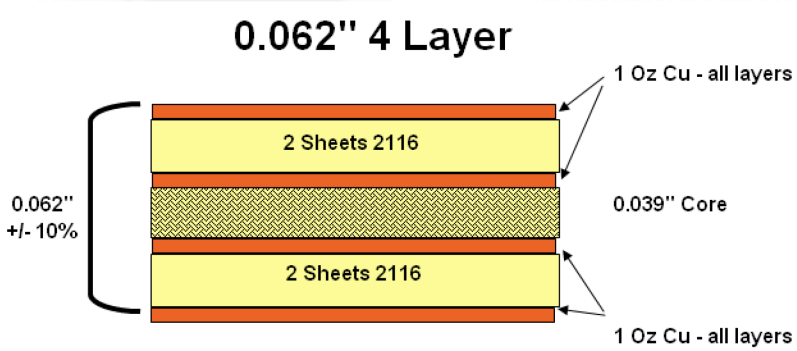


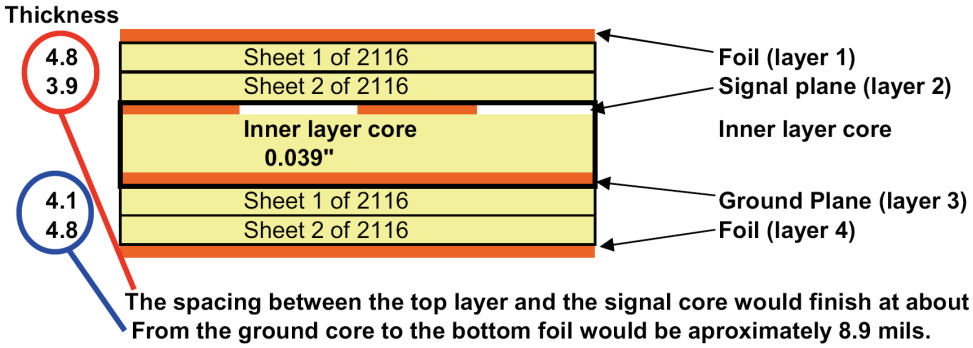
Figure 3: Typical layer stackup of 4 layer, 0.062" thick circuit board.

The chart below provides the thickness for a single sheet of each type of prepreg after processing through the press. The measurements are in mils. For multiple sheets or mixed packages simply multiply or add the various thickness values.

Prepreg	Over 1/2 oz Cu			Over 1 oz Cu			Over 2 oz Cu		
	Signal	Ground	Foil	Signal	Ground	Foil	Signal	Ground	Foil
106	1.8	1.9	2.0	1.7	1.8	1.9	1.5	1.6	1.7
1080	2.4	2.6	2.8	2.3	2.5	2.8	2.1	2.3	2.6
2116	4.0	4.2	4.9	3.9	4.1	4.8	3.9	4.1	4.6

= The signal category represents a sheet of prepreg in contact with copper area of 50% or less.
= Ground represents a sheet in contact with copper coverage in excess of 50% of the board area.
= The foil column is for a prepreg sheet that is in contact with the outer layer foil.

The stackup for our standard 0.062" 4 layer with one ground and one signal plane using 1 oz Cu and two sheets of 2116 pregreg on each side of the core would look like this:



The spacing between the top layer and the signal core would finish at about 8.7 mils
From the ground core to the bottom foil would be aproximately 8.9 mils.
Add to that the core thickness of 0.038 & the four layers of 1 ounce Cu at 1.35 each

Cu	**4 x 1.35**	**5.4**
Core		**39.0**
Prepreg top		**8.7**
Prepreg bottom		**8.9**
		62 Finish +/- 10%

The values listed on this page are nominal and variations may occur due to various environmental mechanical and/or design conditions.

Figure 4: Sheet used to obtain dielectric thickness (provide by Advanced Circuits)

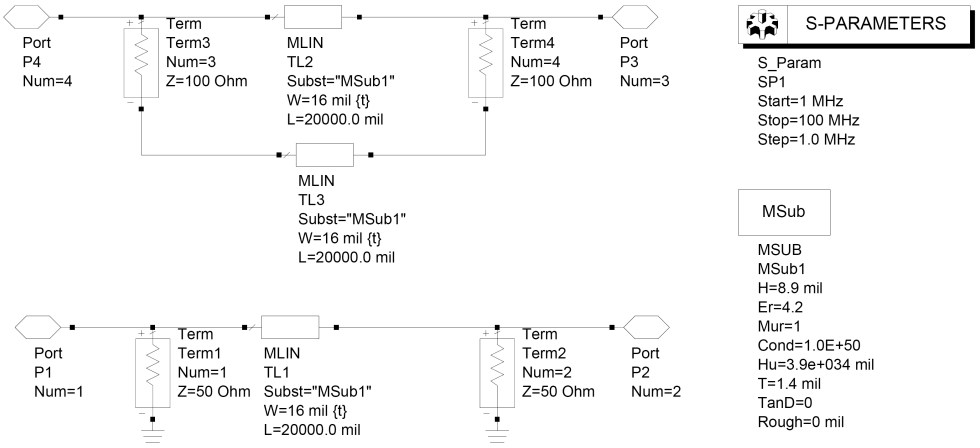


Figure 5: ADS circuit simulating 100 Ω differential and 50 Ω single-ended transmission line impedance.

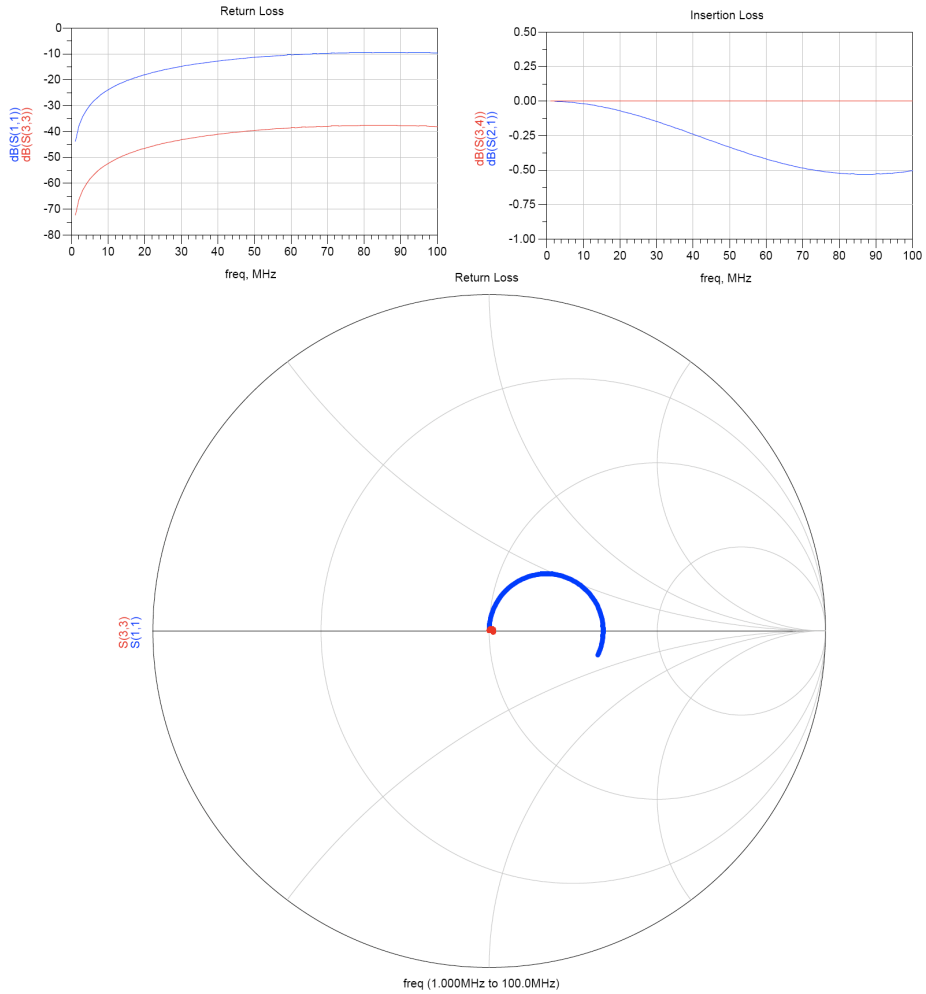


Figure 6: Results of ADS simulation. 20” microstrip transmission line using the above parameters for two trace widths, 8 mils (Blue) and 16 mils (Red).