LWA-SV Station Architecture
Ver. 1

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1 Introduction

1.1 Purposes

This document serves to describe the as-built architecture for the Long Wavelength Array station located on the Sevilleta National Wildlife Refuge (LWA-SV). This supplements what is found in Cranmer et al. [4] and parallels the contents of the original LWA Station Architecture document (LWA Memo 161 [1]) in that it describes the design and specifications for LWA-SV. It should be noted that for some subsystems only variances from LWA1 are noted rather than exhaustive list of feature and specifications provided.

1.2 Terminology and Acronyms

From the original LWA architecture document:

> The LWA is an array of stations which collectively operate as an interferometer. Each station has an array of antennas which are used to form beams. Thus, the use of the word "array" in LWA discussions can sometimes be ambiguous. In this document, the word "array" always refers to the antennas that are part of the station and which are used to form station beams, unless explicitly indicated otherwise.

The naming conventions used in this document largely follow those of in LWA Memo 161, Table 1 with one notable exception. LWA-SV is based on the Advanced Digital Processor (ADP; Cranmer et al.) rather than the original Digital Processor (DP) used at LWA1. Table 1 lists the nomenclature associated with ADP. It should also be noted that this change in the digital backend is likely to be the same for all stations built after LWA1.

Section	Nomenclature	Subsystem	Remarks
	ADP	Advanced Digital Processor	
4.1	ROACH2	F-engine	
4.2	DRX Pipeline		
4.2.1	BFU	Beamformer	
4.2.2	COR	Wideband correlator	
4.2.3	TBF	Transient Buffer – frequency domain	TBW-like data product for ADP
4.3	TBN Pipeline		
	TBN	Transient Buffer – narrowband	
4.4	T-Engine Pipeline		
	DRX	Digital Receiver	
	MCS	Monitoring and Control System	
	PCD	Power Conditioning and Distribution	
	EMD	Electromechanical Design	

Table 1: Subsystem hierarchy and nomenclature where it differs from LWA1.

1.3 Specifications

Table 2 provides the operational specifications of LWA-SV. Those items under the "Domain" category define requirements that apply to all other aspects of the station.

Specification	Name	Value	Remarks
Domain			
Max integration time	τ_{max}	8 h	Same as LWA1
Min Frequency	ν_{min}	3 MHz	For ionospheric work
Max Frequency	ν_{max}	88 MHz	
Sky Coverage	Ψ	$z \leq 74^\circ$	z is zenith angle
Other			
Number of stands	N_a	256	Includes one outrigger for calibration
Beam size	ψ	$8^\circ(20\text{MHz}/\nu)$	Full width at half maximum
Number of tunings	N_t	2	All beams share the same frequency setup
Number of beams	N_b	2	Each with 2 orthogonal pols
Polarization		dual circular $\leq$ 10 dB	cross-polarization isolation
Instantaneous bandwidth	B	19.6 MHz	via DRX, adjustable downward
		39.6 MHz	via TBF when both tunings are combined
Finest Temporal Resolution	Δt	25 ns	via TBF ($= 1/B$)

Table 2: A simplified subset of specifications for LWA-SV.

2 Array Subsystem (ARR)

The array subsystem (antennas, ground screen, and front end electronics) is the same as for LWA1. See LWA Memo 161 [1], Section 2 for a detailed description of this subsystem.

3 Analog (RF) Signal Path

The analog signal path consists of the front end electronics (FEE), RF and power distribution (RPD), shelter entry panel (SEP), and analog receiver (ARX) subsystems. Along this path the signal output from the antenna is transported to the shelter, amplified, and filtered to approximately the frequency range of interest $[\nu_{min}, \nu_{max}]$ from Table 2. These four subsystems are the same as what is defined in LWA Memo 161 with the exception of ARX. The changes to ARX are detailed below.

3.1 Analog Receiver (ARX)

ARXs are subsystems which are part of the ASP subsystem, and provide the additional gain and selectivity required for input to the digitizer.

LWA-SV uses Revision G ARX boards and an example board is shown in Figure 1. These differ from the boards at LWA1 in several aspects:

1. Reduced Common Mode Pickup – The MMCX daughterboard and long input traces on the LWA1 boards has been removed in favor of MMCX connectors located near the front of each signal path. Since this moves the connectors across one of the long edges of the boards, short MMCX–MMCX pigtails with a right angle connector on one end are used to group the signals together and access them from the front edge of the board (see Figure 1).
2. Removal of Electromechanical Relays – The electromechanical relays on the LWA1 boards that physically disconnected each signal path when the board was unpowered have been removed in favor of protection diodes.
3. Coherent Signal Injection – The ARX boards at LWA-SV have a signal splitter and power couplers on the board that allows for coherent tone injection into the signal paths after the

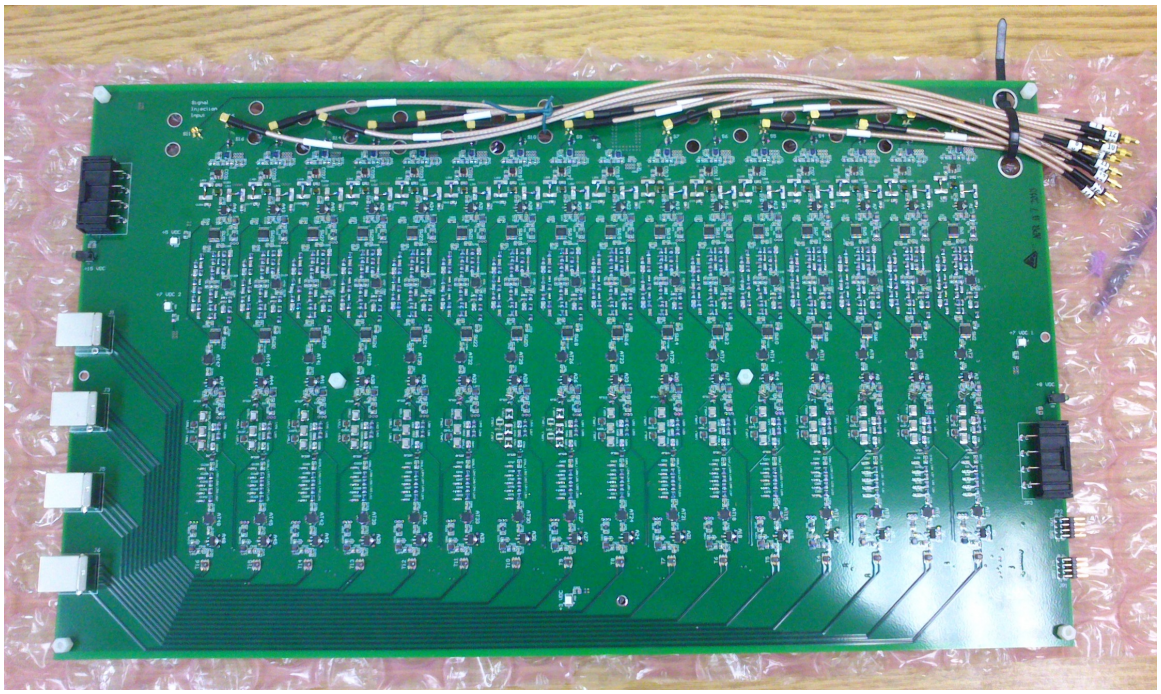

Figure 1: Picture of an ARX Rev. G board with the MMCX–MMCX pigtails installed at the input of each signal path.

Bias-Ts. This was added to as a way to deal with the digitizer startup ambiguity in the ROACH2 boards (see Section 4.1).

4. FM Notch Filter – The FM notch filter has been moved from the end of the signal chain to before the first amplification stage to improve FM rejection. This, however, had the unintended consequence of increasing ripples in the antenna spectra due to reflections between this filter and the front end. To counteract this a 9 dB pad was added between the filter and the Bias-T to damp the reflection. This reduces the effective maximum gain of the board to +59 dB.

5. Low Frequency Cutoff – The Rev. G boards have an additional switchable signal path after the split bandwidth/reduced bandwidth chain that allows for operation down to 3 MHz. These lower frequency versions of the filters are typically denoted by appending a "@ 3MHz" to the end of the filter name. Thus, there are five analog filter modes at LWA-SV:

   (a) Split Bandwidth,
   (b) Full Bandwidth,
   (c) Reduced Bandwidth,
   (d) Split Bandwidth @ 3 MHz, and
   (e) Full Bandwidth @ 3 MHz.

   The frequency response of each filter is plotted in Figure 2.

4 Digital Signal Path

The digital signal path includes portions of the ADP, MCS-DR, and DAC subsystems. Within the ADP subsystem, ARX output is digitized by ROACH2 boards and distributed to BFUs and TB(s).

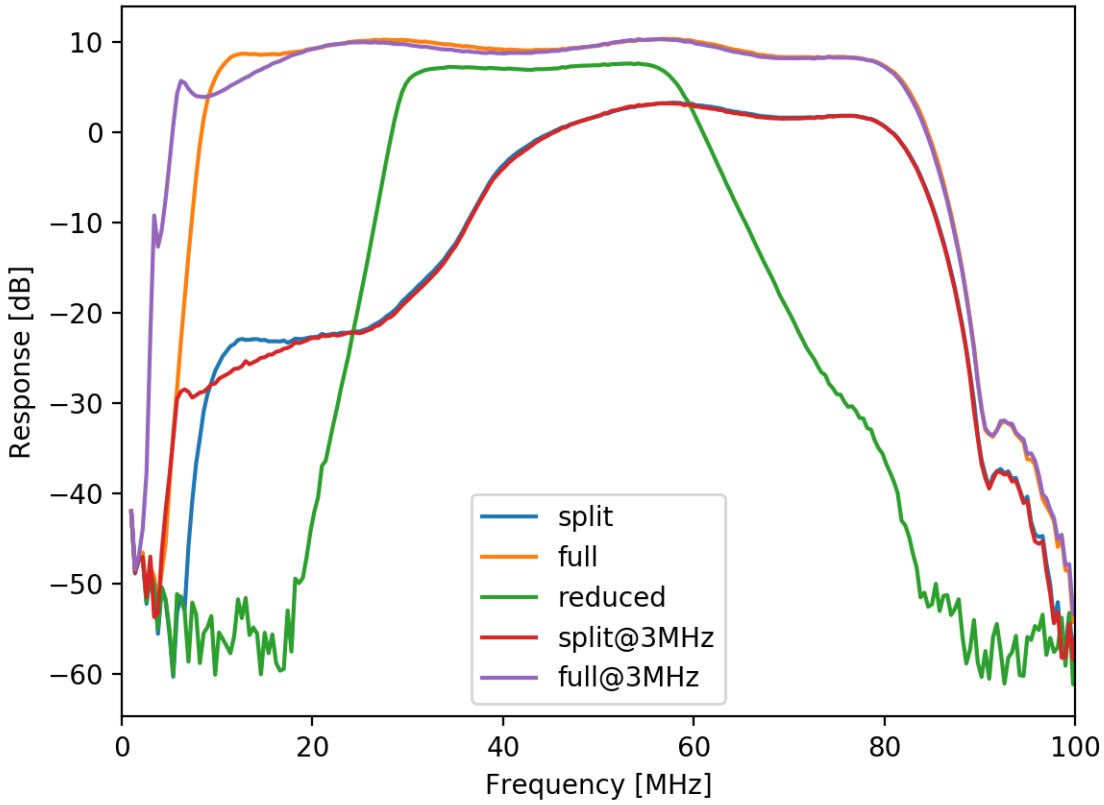

Figure 2: Example ARX Rev. G filter responses as a function of frequency.

BFU outputs are conveyed to the DRX subsystems, and then to DAC (or in LWA1 and LWA-SV, MCS Data Recorders). An overview of the processing framework and design of the ADP subsystem is provided in Cranmer et al. [4].

4.1 ROACH2 Boards

The ROACH2 boards[1] serve as the F-engine for the ADP subsystem and the firmware is described in LWA Memo 213 [7]. These boards digitize the signals from the ARX boards using two ADC16x250-8 digitizer boards[2], covert the data into the frequency domain using a 8,192 point FFT, and transmit the complex spectra data via 10 GbE UDP multicast with a SFP+ mezzanine card[3] (Figure 3).

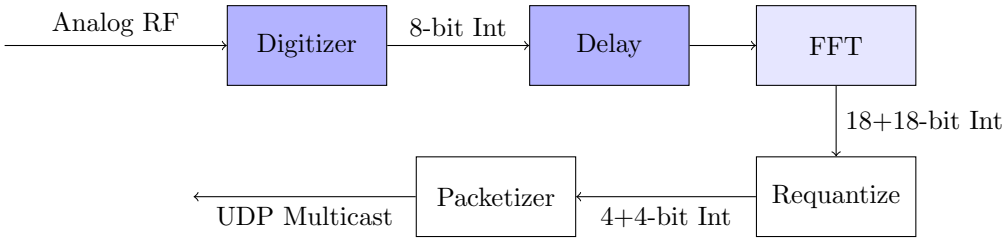

Figure 3: F-Engine diagram based on LWA Memo 213 [7]. The data are in the time domain until the FFT (blue blocks). After the FFT the data are in the frequency domain (white blocks).

Since each ADC16x250-8 board can process 16 inputs (four inputs per digitizer) at the LWA-SV sample rate of 204.8 MHz, each ROACH2 handles 16 dual polarization antennas. The ADC16x250-8 digitizer cards are based on the Hittite HMCAD1511 digitizers which have a sample startup ambiguity. Briefly, when the four digitizer chips are brought up on each digitizer card they are within ± 1 sample of each other, depending on the exact timing of when each of the chips is brought up relative to the edge of the synchronization pulse. To resolve this ambiguity the ADP subsystem provides a 30 MHz calibration tone that is coherently injected to the signal path via the ARX boards. Measurements of the phase of the tone across the different ADCs are uses to apply a compensating delay in the ROACH2 firmware.

After the data is converted to the frequency domain, all subsequent processing is done using the seven computing nodes of the ADP subsystem. The computing is divided into three parts: the DRX pipeline, the TBN pipeline, and the T-Engine pipeline.

4.2 DRX Pipeline

The DRX pipelines run on six of the seven servers, and each server receives one sixth of the total bandwidth transmitted by the ROACH2 boards for each tuning. Thus, there are a total of 12 DRX pipelines running at the station. The DRX pipeline is responsible for the TBF and COR data products as well as the intermediate BFU data product that is used by the T-Engine.

4.2.1 Beamformer Unit (BFU)

The BFU in the DRX pipeline is implemented using the Bifrost `bifrost.linalg.LinAlg` module. This performs a matrix multiply that multiples the beamforming coefficients received from the station

[1] `https://casper.ssl.berkeley.edu/wiki/ROACH2`
[2] `https://casper.ssl.berkeley.edu/wiki/ADC16x250-8_RJ45_rev_1`
[3] `https://casper.ssl.berkeley.edu/wiki/SFP+`

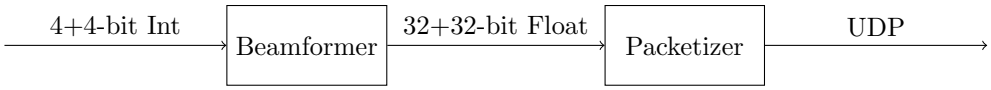

Figure 4: BFU block diagram. The data are in the frequency domain and the color coding is the same as in Figure 3.

MCS through "BAM" commands by the 4+4-bit complex integer data from the F-Engine data. The result of this is four beam-polarization pairs that are represented as 32+32-bit complex floating point numbers with the same time resolution as the input data. This intermediate beamformed product is then sent to the T-Engine pipeline for further processing and conversion back into the time domain (Figure 4).

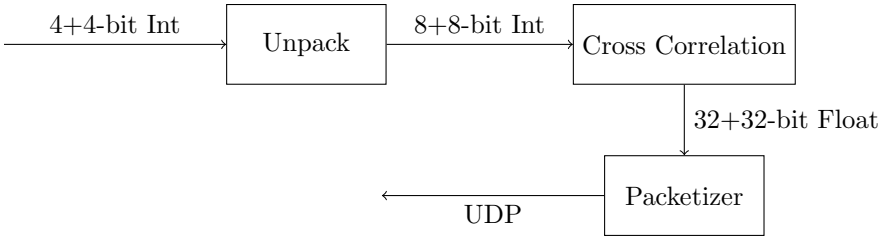

Figure 5: COR block diagram The data are in the frequency domain.

4.2.2 Wideband Correlator (COR)

The COR mode is also implemented using the Bifrost `bifrost.linalg.LinAlg` module. This mode first unpacks the 4+4-bit complex integer data to 8+8-bit complex integers and then multiplies the data by the Hermitian product of itself to form 32,896 baselines and autocorrelation products with full linear polarization (XX, XY, YX, and YY) as 32+32-bit complex floating point numbers. These products are then accumulated for 5 s before they are packetized and transmitted out of ADP (Figure 5). The data are currently sent to the Orville Wideband Imager which is described in [2]. It should be noted that the COR data is only output from the first tuning at the station and, therefore, the bandwidth available is limited to ≈20 MHz.

4.2.3 Transient Buffer – Frequency Domain (TBF)

The TBF mode is a frequency domain version that is similar to TBW at LWA1 in that it provides more bandwidth than is available with TBN but with a lower duty cycle. Since the TBF data comes from the same pipeline as the BFU, its frequency setup is governed by what the beamformer has been set to. The TBF buffer is approximately 5 s in size but dumps of only 1 to 2 s have been tested. The output data are complex spectra from all antennas stored as 4+4-bit complex integers and are transported via UDP multicast. The duty cycle of this mode is such that it takes approximately 60 s to write out 0.1 s of data, or about 0.2%.

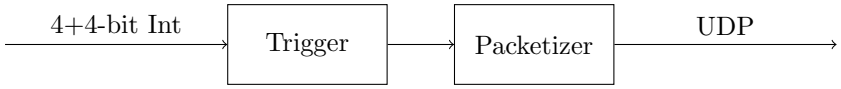

Figure 6: TBF block diagram. The data are in the frequency domain and the color coding is the same as in Figure 3.

The TBF mode is also the basis for the lightning self-triggering feature available on the ADP subsystems. Briefly, this mode examines the mean power seen on stands 3, 116, and 248 (which roughly form an equilateral triangle that spans the array) and looks for peaks that occur across all six server within 500 μs of each other. Triggers that meet these two criteria trigger a TBF dump that is written to disks on ADP. This mode has been used for studying the ionosphere with lightning by Malins et al. [6].

4.3 TBN Pipeline

The TBN pipelines run on the same six servers as the DRX pipeline but with only a single instance per server. The TBN data stream from the ROACH2 boards is also different in that the TBN pipeline only receives 200 kHz of bandwidth from three ROACH2 boards (48 stands) on each server. The TBN pipeline takes in the 200 kHz of bandwidth, decimates it according to the filter code set by a "TBN" command, performs and inverse FFT to move the data back into the time domain, perform sub-channel tuning with a phase rotator, filter the data to set the bandpass, and then packetizes the data. The packetized data are complex voltage time series stored as 8+8-bit complex integers. Similar to TBF, the data are transported via UDP multicast (Figure 7).

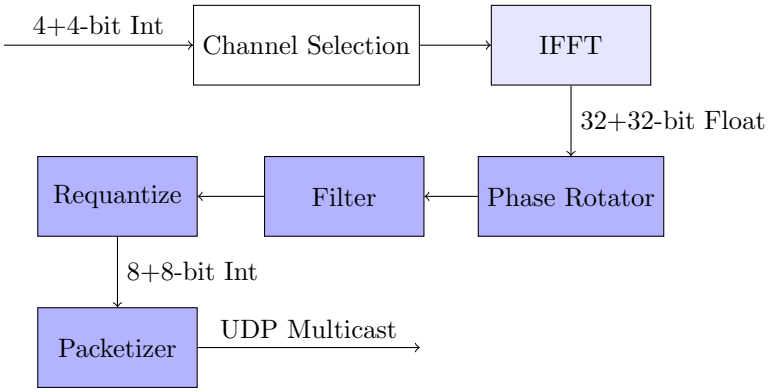

Figure 7: TBN block diagram. The data are in the frequency domain until the IFFT. After the IFFT the data are in the time domain. The color coding is the same as in Figure 3.

4.4 T-Engine Pipeline

The T-Engine pipelines run on the ADP headnode and aggregates the intermediate beamformed products from the DRX pipeline BFUs in order to generate DRX data. Two T-Engine pipelines are used for standard operations, one for each tuning. The pipelines receive the intermediate beamformed data, perform an inverse FFT to get the data back into the time domain, perform sub-channel tuning with a phase rotator, filter the data to set the bandpass, and then packetize it. The output data are complex voltage time series stored as 4+4-bit complex integers. Similar to TBN and TBF, the data are transported via UDP multicast.

5 Timebase and Clock Distribution

The Timebase and Clock Distribution (TCD) subsystem at LWA-SV is similar to that at LWA1 but with two notable exceptions. The first is that the TCD has a second programmable clock that is cabled into the ARX boards as part of the coherent signal injection need to calibrate the startup

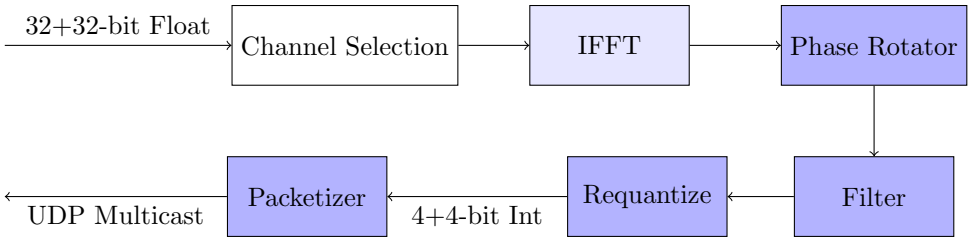

Figure 8: T-Engine block diagram. The data are in the frequency domain until the IFFT. After the IFFT the data are in the time domain. The color coding is the same as in Figure 3.

state of the digitizers in ADP (see Section 4.1). Second, the main station clock rate is 204.8 MHz instead of the 196 MHz at LWA1. This increased clock rate is needed to get a channel width of 25 kHz from the F-Engine.

6 Alternative Backends

The UDP multicast data products from the ADP subsystem enable multiple backends to run commensally without interfering with the operation of LWA-SV. There are currently three such systems in operation:

1. The E-Parallel Imaging Correlator – This uses the raw F-Engine data to make high time resolution (∼ms) all-sky images. See Kent et al. [5] for details. This system is currently under development.
2. The LWA All-Sky Imager – This shares the TBN data stream with the TBN data recorder to making all-sky images with 100 kHz of bandwidth and 5 s integration times.
3. The Wilbur Single Dispersed System – This shared the DRX data stream for beam 1 to run realtime searches for single dispersed pulses. This system is described in [3] and is currently under development.

Other systems can potentially be added within the constraints of the available data switch bandwidth, number of free ports on the data switch, and the added power and heat loads. It should also be noted that all of the alternative backends listed above are located in the UNM SERF building located on the refuge about 500 m north of the LWA-SV site.

7 Shelter (SHL)

The electronic shelter for LWA-SV is similar to that at LWA1 with five exceptions:

1. The HVACs have a "low ambient control" installed that should help prevent icing up when the outside temperature is low. It is not clear that this add-on actually helps.
2. A custom HVAC controller interface board has been installed to help monitor the state of the HVACs and to provide a mechanism to remotely de-ice the station. This feature has since been installed at LWA1 as well.

3. The air handling inside the shelter is now ducted through a raised floor to help keep the cold and warm air separated. Each rack sits over an opening the floor and a bypass is installed near the SEP to prevent over-pressurizing of the floor.

4. The doors that cover the SEP on the outside of the shelter have been fitted with adjustable vents to help control moisture that might accumulate inside the SEP.

5. Additional 240V receptacles were installed after delivery of the shelter.

8 Site & Infrastructure for LWA-SV (SIT)

The array layout of LWA-SV is the same as LWA1 although the topography of the land is different and not as flat (there is a central hump that runs roughly north-south through the middle of the array). At LWA-SV it was decided not to use conduit for running the coaxial cable to the antennas; instead the cable has been direct buried. The outrigger at LWA-SV is also located approximately 300 m west of the array.

9 Document History

- Version 1 (Aug 31, 2020): First version.

References

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[7] D. Price, "LWA-SV F-Engine Firmware Overview", Ver. 1, Long Wavelength Array Memo 213, Feb 22, 2017, [online] `http://www.phys.unm.edu/~lwa/memos/index.html`.