# LWA DRX High-level Design - v0.2

Johnathan York

December, 2007

# 1 Introduction

This document presents a preliminary design for the LWA digital receiver (DRX) module, and also presents some details for how multiple DRX modules can be chained together to form the DP2 subsystem. The larger context and requirements for this design can be found in the LWA System Architecture document [1], and the LWA System Technical Requirements document [2]. The LWA digital receiver (DRX) module is responsible for providing frequency selectivity within the LWA station digital signal processing chain. Each DRX consists in part of two parallel paths, corresponding to 2 simultaneous tunings  $\nu_1$  and  $\nu_2$ . In each path, a single spectral swath of width B (currently 8 MHz, as specified by LWA TR-2) is selected from the digital passband, divided into smaller contiguous channels of width  $\Delta \nu$  (currently 100 Hz, as specified by LWA TR-3), and sample rates are adjusted appropriately.

## 2 Interfaces

Architecturally, the digital receiver (DRX) module resides within the DP2 subsystem, receiving input from an attached beamforming unit (BFU) and providing output to the data aggregation and communications (DAC) subsystem. The DRX context and interface connections are shown in Figure 1

#### 2.1 Mechanical/Power/RFI Interfaces

Each DRX module is expected to be a 19" rack-mountable device, no deeper than 22", and of a height of approximately 3U. Power shall be supplied via 110V 60 Hz AC on a standard connector located on the rear of the DRX module. Power dissipation shall be <200 Watts per DRX, and sufficient upward directed airflow is expected to exist within the rack to remove this heat. Each DRX module will be independently rack-mountable, and there will be no specific packaging around the DP2 subsystem as a whole, but instead the collection of DRX modules are anticipated to form the DP2 subsystem inside of racks located within the shelter.

As detailed in [3], the mechanical interface for the input from the BFU and the DP2 daisychain output will be provided over Infiniband connectors exposed on the front panel of the DRX module. The timing epoch signal shall be provided via 50 ohm BNC connector located on the front panel of the DRX module. The interface to the MCS shall be provided over two male DB9 connectors located on the front panel of the DRX. The front panel of the DRX shall also contain,



Figure 1: DRX Context Block Diagram

at minimum, LEDs to indicate: power, 1PPS heartbeat to indicate FPGA operation, and LEDs to indicate data-good on each of the input links.

Because the DRX modules will be located inside shielded racks inside of the station shelter, shielding to limit radiated RF emissions is best handled physically outside the DRX module. Nevertheless, the overall required incidental RF emission levels for the entire LWA shelter will almost certainly require that each DRX module be a "good RF citizen". To provide a reasonable interface for engineering the various layers of RF shielding, it shall be required that each DRX module in isolation (with I/O ports covered with copper tape) meet FCC part 15(a) incidental emissions level. It is expected that the racks and shelter of the LWA module will provide sufficient shielding to meet LWA technical requirement TR-24C. This level is established based on the reasoning that COTS rack-mount computers, which are engineered to meet FCC part 15(a) are likely to be shielded in the same rack as the DRX modules, such that this level forms a reasonable RF emissions goal for the DRX.

### 2.2 BFU Interface

The BFU Interface is responsible for providing time-domain samples into the DRX. The interface will largely follow that documented in the DP1 Daisy Chain Preliminary Interface Control Document [3], with the following modifications:

- A 343 MHz LVDS clock will be generated by the BFU, and delivered to the DRX alongside the 4 LVDS data lanes.
  - This clock will be coherent with the data lanes with edges aligned to the data within 1/8th of a bit period, and will be used by the DRX to sample the LVDS data lines in a

dual data rate (DDR) fashion

- Behavior of the DRX when this clock is absent shall be undefined
- A word-marker LVDS signal will be generated by the BFU, and delivered to the DRX alongside the 4 LVDS data lanes and clock
  - This signal shall arrive at the DRX with edges coincident with both the data and clock lanes
  - This signal shall have 50% duty cycle and period of 28 clock cycles (24.5 MHz)
  - The first sampled high-value shall be coincident with the first bit of the 28-bit word on all four lanes
- 28-bit data word present on each lane shall be in the following order: [b3 b2 b1 b0 i11 i10 i9 i8 i7 i6 i5 i4 i3 i2 i1 i0 q11 q10 q9 q8 q7 q6 q5 q4 q3 q2 q1 q0 ], where:
  - b3-b0 are the in-band signaling bits defined for the DP1 Daisy Chain ICD
  - i11-i0 are the signed in-phase sample components (2's complement notation)
  - q11-q0 are the signed quadrature sample components (2's complement notation)
- The four data lanes shall be numbered 0-3, with data words transmitted for samples n,n+1,n+2, and n+3 transmitted simultaneously on lanes 0,1,2, and 3 respectively.
- The 12-bit real-valued "RAW ADC samples" mode (signaling word b1=1,b2=1) will not be supported. Behavior of the DRX in this mode shall be undefined.
- The Gold code (b3) signal from 32 consecutive 28-bit words shall be captured by the DRX and the resulting 32-bit word used to time tag the data. Otherwise the (b3) signal shall be ignored.
- The common mode voltages on the LVDS lines shall not exceed the range of 1.0-2.0V from the local DRX ground.
- The signal scheme specified here requires 6 LVDS lanes (4 data + 1 clock + 1 word marker), and so placing data for both polarizations on a single Infiniband cable as suggested in [3] may require using 12X cables rather than 4X cables.

To implement the DP2 daisy chain, each DRX module shall be responsible not only for receiving data via this interface, but providing an unmodified duplicate of the data for connecting to the next module in the DP2 daisy chain.

#### 2.3 DAC Interface

The DAC interface is responsible for providing the output of the DRX to the DAC subsystem. The output from a single polarization of the DRX shall be carried through a unidirectional, single lane, Aurora-protocol based transport delivered via LVDS and clocked at 1960 Mbit/s. The data shall be present in frames beginning with an 8b10b comma character K.28.7, followed by data values, and padded by 8b10b idle character K.23.7. The payload format shall consist of the fields shown in Table 1.

Mnemonic	Bytes	Description
frame_marker	1	Frame Marker = hex $5A$
$\operatorname{prot}_{\operatorname{version}}$	1	Protocol Version = hex $01$
flags	1	Bit-field [000000 data_valid counters]
$fft_len$	1	FFT-length $(2^{**}n)$ ; currently fixed at hex 12
drx_state	2	Bit-field containing DRX state [enable deci2 deci1 deci0 0 0 $$
		freq9 freq8 freq7 freq6 freq5 freq4 freq3 freq2 freq1 freq0]
$\mathrm{fft}_{-\mathrm{accum}}$	2	Number of FFT intervals accumulated for this frame
$mcs_tag$	8	MCS Tag (use to be defined by MCS)
$frame_cnt$	4	Frame counter, increments by 1 each output frame
gold_code	4	32-bits of captured Gold code values, with last bit coincident
		to first sample value used to compute this frame
payload	32768	$4096$ little-endian values: If fft_accum=0, these are 32-bit
		signed complex values; If fft_accum!=0, these are 64-bit un-
		signed real values

Table 1: DRX Output Packet Payload Format

Data rates can be estimated assuming the parameters shown in Table 2.

If the FFT input bit-depth is 16 bits, a 4096 point FFT produces a  $16+\log_2(4096)+1=29$  bit output word. Therefore in the case where the DRX is used purely for channelization and not detection it is sufficient to output 32 bit values from the FFT. In the worst case of a first-stage tuning decimation ratio of 8, it will be necessarily for each DRX to output 8,192 32-bit values 2,990 times per second. This results in a data rate of approximately 784 mbit/s/tuning/polarization. Given that each DRX modules is expected to provide 2 tunings on 2 polarizations, the output data rate from a single DRX module could exceed 3.1 gbps. For this reason, each tuning and polarization will be output on a separate LVDS lane, each clocked at 1980 MHz.

### 2.4 MCS Interface

The MCS interface is responsible for providing command and control information to the DRX, and for accepting status telemetry from the DRX.

The required control parameters are outlined in the *Operating Modes* section of this document, and are detailed in Table 4. The size of these parameters total to approximately 90 bits of state information per polarization per tuning. Thus each DRX module contains approximately 360 bits of configurable state information.

The DRX is also responsible for providing telemetry to the MCS. This information shall consists of the fields outlined in Table 3. For brevity, the telemetry is shown for only a single tuning and polarization. Thus for 2 polarizations and tunings, the fields shown shall be replicated 4 times per DRX module resulting in approximately 392 bits of telemetry per update.

The command and control electrical interface between the DRX and MCS shall be through two 115200 baud RS232 interfaces exposed as two DB9 connector on the DRX enclosure. Each polarization shall be assigned to a separate physical DB9 connector, thereby resulting in two signal paths associated with two tunings controlled over a single DB9 connector. The precise serial protocol will be elaborated in a later document, however it is expected that parameter updates

Parameter	Value	Units
Input clock	196	MHz
First stage tuning decimation ratio	8 - 256	
FFT Length	4096	bins
Number of FFTs per second	93-2990	FFTs per sec
Maximum accumulation period	1	second

Table 2: DRX Parameters Relevant to Computing the Output Data Rate

will be sent to the DRX via RS232, and those changes will take effect upon the MCS sending an epoch pulse, which shall be a 3.3V CMOS signal provided from the MCS to the DRX via a BNC connector mounted on the exterior of the DRX module.

### 2.5 Operating Modes

For each polarization and tuning, the DRX shall have 5 operationally configurable parameters shown in Table 4.

While both tuning frequency and accumulate&dump interval are programmable, the primary modal aspect of operation revolves around the tuned bandwidth. Six bandwidth modes are provided, and are detailed in Table 5.

# 3 Major components

A block diagram showing the major components of the DRX DSP chain can be found in Figure 2. Each of the major components are detailed in the remainder of this section.

#### 3.1 First Stage Tuner

The first stage tuner is responsible for selecting a desired 8 MHz bandwidth out of the 98 MHz of input bandwidth. The center frequency of the desired band specified by a 10-bit integer that is in units of a base frequency of 98 MHz/1024 or approximately 95.7 kHz. This provides tuning granularity sufficient to place the intended center frequency within the center 25% of the captured bandwidth, even in the smallest bandwidth operating mode. Moreover, the base frequency being a factor 1024 lower than the 98MHz core clock provides an efficient FPGA implementation utilizing the RAMB16 elements present in Xilinx FPGAs.

### 3.2 CIC Filter

The Cascaded Integrating Comb (CIC) filter [4] is a computationally efficient filter structure composed of only time delays, additions and multiplications. In the LWA DRX, the 8th order CIC block provides two functions: 1) initial filtering of undesired out-of-band signals, and 2) programmable decimation. Programmable decimation is a noteworthy feature of the CIC filter structure that allows a single hardware component to provide several different, but related low-pass filters of varying cutoff frequency. The varying cutoff frequency is required to implement multiple operating modes

Parameter	Description	Bits
inclkpresent	Input clock present on BFU interface	1
wordsyncpresent	Word synchronization present on BFU interface	1
inbandsignals	Inband signaling bits b3-b0 as defined in [3], as sampled from	1
	the incoming data stream	
countererror	If in "counters mode" as defined in [3], 1 if a counting error	1
	been detected, otherwise 0	
lanecountererror	If in "lane counters mode" as defined in [3], 1 if a counting	4
	error been detected on each of the 4 lanes, otherwise $0$	
enable	Operation Enabled	1
freq	Tuned center frequency (specified as multiples of a base fre-	10
	quency of 98 MHz / $1024 = 95.7 \text{kHz}$ )	
deci	First-stage tuning decimation ratio (specified logarithmi-	3
	cally: decimation ratio = $8*2**$ deci)	
accum	Number of FFT intervals to accumulate before dumping	12
	(0=no detection $)$	
$\operatorname{tag}$	MCS-definable tag to be passed transparently into output	64
	data stream	

Table 3: DRX Telemetry (per tuning, per polarization)

with differing bandwidths used satisfy the DRX requirements of maximum bandwidth (B=8 MHz), and frequency resolution ( $\Delta \nu <=100$ Hz).

The required CIC register lengths can be computed via the equation  $B_{out} = B_{in} + N \log_2 R$ , where

- $B_{out}$  is the number of bits required at the output,
- $B_{in}$  is the number of bits provided at the input,
- N is the CIC filter order (8),
- R is the decimation factor (2,4,8,16,32, or 64 depending on operating mode).

For the LWA DRX, an 8th order filter operating in the worst-case operating mode (64X decimation) on 16-bit input data, the CIC registers will need to be 64-bits in length.

## 3.3 FIR Filter

The Finite Impulse Response (FIR) filter block is a digital low-pass filter structure used to filter out undesirable out-of-band signals and decimate the signal by 4X to reduce downstream processing requirements. The 64 coefficients are quantized to 16-bits and are designed with the Remez exchange algorithm. Passband ripple is limited to less than 0.1 dB, while alias suppression exceeds 86dB. The FIR filter response is shown in Figure 3.

The composite CIC and FIR filter response for each of the 6 operating modes is shown in Figure 4. The passband is largely monotonic, rolling off < 0.6 dB to the edge of the passband, with ripples

Parameter	Description	Bits
enable	Enable operation	1
freq	Tuned center frequency (specified as multiples of	10
	a base frequency of 98 MHz / $1024 = 95.7$ kHz)	
deci	First-stage tuning decimation ratio (specified	3
	logarithmically: decimation ratio = $8*2**$ deci)	
accum	Number of FFT intervals to accumulate before	12
	dumping $(0=$ no detection $)$	
$\operatorname{tag}$	MCS-definable tag to be passed transparently	64
	into output data stream	

 Table 4: DRX Operating Parameters (per tuning, per polarization)

limited in magnitude to <0.1 dB. The filter stopband provides alias rejection exceeding 94 dB in the worst-case operating mode, with narrower operating bandwidth modes providing substantially more rejection far from the tuned frequency.

#### 3.4 Polyphase Filter Bank

Although technically a "polyphase filterbank" (PFB) refers to a specific multirate filter implementation structure, within the context of radio astronomy it has come to refer the use of such a structure to implement the channelization of time-domain data into the frequency domain. This usage arises out of the dominant application of the PFB structure, which leverages the Fast Fourier Transform (FFT) to efficiently implement a set of M related N-length finite impulse response (FIR) filters on the same input data stream. To utilize a FFT-based PFB, the set of FIR filters implemented must be complex frequency shifted versions of each other, with the frequency steps uniform and evenly divided across the Nyquist band. Restated in the context of frequency channelization, M is the number of frequency channels while N is the length of the FIR filter implemented which is related to factors including interchannel isolation.

As is typical with FFT-based algorithms, a particularly simple and efficient implementation is possible with M restricted to a power of 2. Furthermore, the PFB structure is simplified and computational efficiency maximized when N is an integer multiple of M. For the LWA DRX, the polyphase filterbank is chosen the have N=32768, and M=4096. That is, the polyphase structure consists of 4096 subbanks each of which are 8-tap FIR filters specified with 16-bit signed coefficients.

The filterbank coefficients implement a low-pass filter with critical overlap and are designed via the classical windowing technique using a Blackman window. A subset of 8 adjacent filterbank responses are plotted in Figure 5. The designed filter provides >75dB suppression one FFT bin distant, and >100 dB suppression two FFT bins distant.

# 4 Computational Resource Estimate

In order to roughly gauge the computational burden it is useful to tabulate both the memory required and multiplications needed per complex input sample. Such an analysis is shown in Table 6. Based on this accounting, a single polarization, single tuning of a DRX will require approximately

deci	Total CIC+FIR Decimation Ratio	$B_{Total}$ (MHz)	$B_{Usable}$ (MHz)	$\Delta \nu \ (\text{kHz})$
0	8	12.250	8.167	2.991
1	16	6.125	4.083	1.495
2	32	3.063	2.042	0.748
3	64	1.531	1.021	0.374
4	128	0.766	0.510	0.187
5	256	0.383	0.255	0.093

Table 5: Bandwidth Modes For LWA DRX

39.25 multiplications per input sample, and approximately 1.7 mbits of RAM. This level of computational ability is readily available in COTS FPGAs, for instance the Xilinx XC5VSX50T, which contains 4.7 mbits of RAM, and 288 18-bit multipliers, and sells for approximately \$958 in small quantities as of November, 2007.

A suitable evaluation board, Xilinx part number HW-V5-ML506-UNI-G is available for prototyping for this FPGA at a cost of \$1,195. Among other features, this board includes Xilinx XC5VSX50T FPGA and exposes 16 LVDS pairs, 32 single ended I/Os, an RS232 port, and a multi-gigabit transceiver interface. The DP2 daisy chain interface outlined above requires 6 pairs, such that 12 pairs are needed for providing input from a BFU and providing the DP2 daisy chain output.

## 5 Issues to be Addressed in Future Versions of this Document

- Reconcile station architecture document's call for 2 parallel tunings per beam with technical requirements call for independently tunable beams
- Elaborate on hardware implementation (number and types of internal PCBs, FPGAs)
- Consider potential use of multidrop bus (e.g. RS485) for MCS
- Specify mechanical connector for DAC interface (Infiniband?)

# 6 Document History

- v0.1
  - Initial draft
- v0.2
  - Added DP2 daisy chain requirement
  - Added reference to suitable evaluation board for prototyping
  - Added mechanical interface section
  - Modified document structure to better match BFU design documents (e.g. LWA Memo 108)
  - Added DRX context block diagram

Single polarization, Single tuning Path



Figure 2: DRX Digital Signal Processing Components for a Single Polarization and Tuning

# 7 References

[1] Ellingson, S. "LWA Station Architecture Ver 0.6," October 9, 2007.

[2] Janes, C. "The Longwavelength Array System Technical Requirements," Draft 9, November 19, 2007.

[3] Ellingson, S. "DP1 Daisy Chain Preliminary Interface Control Document v0.1," September 18, 2007.

[4] Donadio, M. "CIC Filter Introduction". July 18, 2000.



Figure 3: Decimating FIR Filter Response



Figure 4: Composite CIC and FIR Filter Response for each of the 6 operating modes



Figure 5: Polyphase Filter Bank Response (4096 Channels, 8 tap subbanks, Blackman Window)

Component	Multiplies/inp. sample	16-bit RAM Words	Notes
Tuner	4	1024	
CIC	0	128	Requires 16 64-bit accumulators for
			each I and Q
FIR	16	192	64 MACs for each I and Q every
			8 input samples (CIC decimates by
			2X, FIR by $4X$ ), $64$ taps stored + $64$
			taps for each I and Q history buffers
PFB-FIR	16	81920	8 MACs for each I and Q input sam-
			ple; 16384 coefficient entries, 32768
			history buffer for each I and Q
PFB-FFT	3	10240	4 mults per radix-2 butterfly, 24576
			butterflies per FFT, FFT executed
			every 32768 input samples; 2048
			twiddle factors, 4096 complex ram
			buffers
Detection	0.25	0	8192 real MACs every FFT, FFT
			every 32768 input samples
Accumulation	0	16384	4096x 64-bit RAM
Total	39.25	109888	

Table 6: Computational resources estimate for a single polarization, single tuning of a DRX in the worst-case bandwidth mode