ADC Candidate Survey

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LWA ADC Candidate Survey

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Introduction

Current LWA plans call for ~52 stations of 256 stands each with 2 orthogonally polarized dipole antennas. As a consequence, LWA will have just over 26,000 independent input signals, requiring a corresponding number of analog−to−digital converters (ADCs). Moreover, the ADC necessarily forms a key link in the receive chain, and therefore limitations of the ADC become limitations in the LWA itself. As a result, it is important to carefully evaluate and select an ADC appropriate for LWA. This memo documents the first step in the selection process, which is a market survey and analysis to identify approximately 3−5 suitable candidates to undergo further evaluation.

Minimum Requirements

As an initial step, it is desirable to develop known characteristics of the LWA into preliminary restrictions on the candidate search space. The minimum requirements detailed in the remainder of this section should be thought of as necessary, but not entirely sufficient, conditions for the ADC to function well for LWA.

Sampling Rate

As the LWA scientific requirements call for coverage of the 20−80 MHz range, and the prevailing wisdom calls for a direct sampling architecture, the Nyquist−Shannon sampling theorem gives us the first naive requirement for candidate ADCs: a sampling rate of at least 160 Megasamples per second (MSPS).

In addition to the theoretical lower bound imposed by the Nyquist−Shannon sampling theorem, several practical considerations are worth noting. First, it is well understood from prior work on LWDA that commercial FM radio broadcasts in the 88−108 MHz band are one of the larger sources of radio interference for LWA. To ensure that a 108 MHz FM broadcast will not alias into the 20−80 MHz range of interest, it is necessary for the sampling rate F_s to be high enough such that F_s−108 => 80. Secondly, in order to relax anti−alias filter requirements, it desirable to add an engineering margin to the theoretical minimum requirements. As a result of these two considerations, the final requirement chosen for the ADC candidate survey process is a sampling rate of 200 MSPS or greater.

Dynamic Range

For the purposes of this paper study, the dynamic range of ADCs can be suitably characterized by two metrics: the maximum Signal−to−Noise ratio (SNR), and the maximum Spurious−Free Dynamic Range (SFDR). These metrics are described in great detail in Analog Devices Application Note 835. Within the context of LWA, one can generally think of SNR as placing a limit on the peak in−band RFI level tolerable while achieving galactic noise limited operation, and SFDR as placing a bound on how much seemingly clean frequency bins can be corrupted by RFI elsewhere in the band. In both cases a larger number is better, and for an application like LWA one generally wants the best SNR and SFDR one can afford. In practice the issue is more complex as SNR and SFDR do not adequately characterize device performance. This elicits the need for detailed lab testing to follow the candidate selection process.

In order to rapidly identify a reasonable lower bound for SNR, daily statistical data from the NRL SpecMaster system located at the LWDA site was examined. An example plot is shown in Figure 1 below.

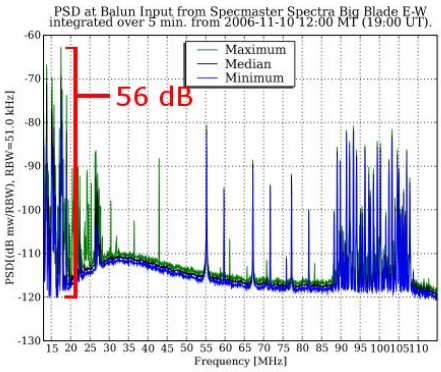

Figure 1: Statistical Plot of NRL data

A quick survey of several days of data showed that the maximum difference between peak amplitude and the average noise floor (or even the lowest amplitude in the graph) in each grouping never exceeded 65 dB. In order to translate this into a useful metric for ADC selection, it is necessary to account for the difference in assumed bandwidth between the SpecMaster and the ADC figure−of−merit. The resolution bandwidth (RBW) given in the SpecMaster data is 51.0 kHz, while ADC SNR is evaluated assuming the Nyquist bandwidth. If we assume a minimum passband of 60 MHz prior to the ADC, we find that the total noise power reaching the receiver is approximately 30 dB higher than the average noise power in the SpecMaster frequency bins. Subtracting this figure from the 65 dB figure discussed earlier, we find the at least 35 dB of SNR is required. However, ADCs are imperfect devices, and experience suggests that ADCs for radiometers should be run with a white noise dither at least 6 dB higher than the natural ADC quantization power level, and that the highest sinusoid should be at least 6 dB below the saturation level. Adding the 12dB of margin required to the 35 dB figure derived earlier gives a minimum SNR requirement of 47 dB.

The maximum achievable SNR for an ADC, as defined in the application note cited above, is bounded by the number of bits output by the ADC. In general, this theoretical bound can be defined by the equation SNR_{dB} <= 1.76 + 6.02 * bits. This implies that we can convert the SNR requirement above into a minimum requirement for the number of bits output by the ADC. In the case of the analysis above, 47 dB SNR implies that the ADCs under consideration must have 8 bits or greater.

Initial Candidate List

In the preceding section, two requirements for the ADC were derived: 1) a sample rate of 200 MSPS or greater and 2) a SNR of at least 47 dB or 8 bits of resolution. A market survey was conducted, and all the ADCs meeting these requirements from Analog Devices, e2v, Maxim IC, Linear Technologies, Texas Instruments, and National Semiconductor were collected and tabulated. In all, 45 devices were examined, each with a sample rate >= 200 MSPS, SNR >= 45 dB, and SFDR >= 60dB. An attached spreadsheet documents detailed parameters for all 45 ADCs meeting these minimum requirements, and the methodology used to derive any needed values.

A summary table of the number of candidate ADCs meeting or exceeding a given minimum sample rate and bit depth is outlined in Table 1.

Table 1: ADC Bit Depth and Sampling Rate

MSPS	8−bit	10−bit	12−bit
200	45	32	20
210	41	31	20
250	28	18	10
300	16	9	4

A more comprehensive review follows below.

ADC Survey Data

The four tables below highlight relevant data from the attached spreadsheet. Although separated primarily for pagination, each table focuses on a distinct aspect of ADCs: Table 2 contains model Information, Tables 3 and 4 contain interfacing information, while Table 5 contains performance information.

Table 2: Model Information

Company	Model	Latest Date	Bits	Inputs	MSPS	Pin Count	Package	Price (1k)
Analog Devices	AD12401	Apr−06	12	1	400	120	Module	525.00
Analog Devices	AD9054A−200	May−01	8	1	200	44	LQFP	19.06
Analog Devices	AD9211−200	May−07	10	1	200	56	LFCSP	32.00
Analog Devices	AD9211−250	May−07	10	1	250	56	LFCSP	39.00
Analog Devices	AD9211−300	May−07	10	1	300	56	LFCSP	46.00
Analog Devices	AD9230−210	Feb−07	12	1	210	56	LFCSP	42.00
Analog Devices	AD9230−250	Feb−07	12	1	250	56	LFCSP	59.00
Analog Devices	AD9410	Jul−07	10	1	210	80	TQFP	53.10
Analog Devices	AD9430−210	Aug−05	12	1	210	100	TQFP	55.00
Analog Devices	AD9480	Apr−05	8	1	250	44	TQFP	16.00
Analog Devices	AD9481	Nov−04	8	1	250	44	LQFP	16.00
e2v (ATMEL)	AT84AS003	Feb−06	10	1	1500	317	EBGA	N/A
e2v (ATMEL)	AT84AD004	Mar−07	8	***2***	500	144	LQFP	N/A
e2v (ATMEL)	AT84AD001	Mar−07	8	***2***	1000	144	LQFP	178.00
e2v (ATMEL)	AT84AS001	May−07	12	1	500	192	EBGA	N/A
e2v (ATMEL)	AT84AS004	Jun−07	10	1	2000	317	EBGA	N/A
e2v (ATMEL)	TS83102G0	Jun−07	10	1	2000	152	CBGA	1,263.00
e2v (ATMEL)	EV8AQ160	Jul−07	8	***4***	5000	380	EBGA	N/A
e2v (ATMEL)	TS83102G0BMGS	Jun−05	8	***2***	500	152	CI−CGA	N/A
	AT84AS008	Nov−06	10	1	2200	152	CI−CGA,CBGA	1,390.00

e2v (ATMEL)								
Linear	LTC2241−10	Jul−07	10	1	210	64	QFN	32.00
Linear	LTC2241−12	Jul−07	12	1	210	64	QFN	42.00
Linear	LTC2242−10	Jun−07	10	1	250	64	QFN	39.00
Linear	LTC2242−12	Jul−07	12	1	250	64	QFN	59.00
Maxim IC	MAX104	Mar−02	8	1	1000	192	ESBGA	199.00
Maxim IC	MAX106	Nov−01	8	1	600	192	ESBGA	125.00
Maxim IC	MAX108	Oct−01	8	1	1500	192	ESBGA	350.00
Maxim IC	MAX1121	Feb−04	8	1	250	68	QFN	17.98
Maxim IC	MAX1123	Feb−04	10	1	210	68	QFN	32.00
Maxim IC	MAX1124	Feb−04	10	1	250	68	QFN	39.00
Maxim IC	MAX1214	Sep−06	12	1	210	68	QFN	54.85
Maxim IC	MAX1214N	Apr−06	12	1	210	68	QFN	41.50
Maxim IC	MAX1215	Sep−06	12	1	250	68	QFN	89.50
Maxim IC	MAX1215N	Apr−06	12	1	250	68	QFN	58.75
Maxim IC	MAX1219	Aug−05	12	***2***	210	100	TQFP	89.25
National	ADC08200	Jul−06	8	1	200	24	TSSOP	7.67
National	ADC08B200	Jun−07	8	1	200	48	TQFP	16.50
TI	ADS5440	Dec−05	13	1	210	80	HTQFP	42.00
TI	ADS5440−EP	Aug−06	13	1	210	80	HTQFP	82.11
TI	ADS5444	Feb−06	13	1	250	80	HTQFP	59.00
TI	ADS5444−EP	Aug−06	13	1	250	80	HTQFP	115.35
TI	ADS5474	Jul−07	14	1	400	80	HTQFP	150.00
TI	ADS5463	Nov−06	12	1	500	80	HTQFP	125.00
TI	ADS5527	May−07	12	1	210	48	QFN	45.00
TI	ADS5547	May−07	14	1	210	48	QFN	82.50

Table 3: Interfacing Information − Power and Digital I/O

Model	Analog Supplies	V_{CC}	Digital Supplies	V_{DD}	Output Levels	Typ. Pwr (*mW*)	SPI Control Port
AD12401	1	3.7	2	3.3, 1.5	LVDS	5700	No
AD9054A−200	1	5	0	−	TTL	640	No
AD9211−200	1	1.8	1	1.8	LVDS	333	Yes
AD9211−250	1	1.8	1	1.8	LVDS	380	Yes
AD9211−300	1	1.8	1	1.8	LVDS	437	Yes
AD9230−210	1	1.8	1	1.8	LVDS	383	Yes
AD9230−250	1	1.8	1	1.8	LVDS	434	Yes
AD9410	2	3.3,5	1	3.3	TTL, CMOS	2000	No
AD9430−210	1	3.3	1	3.3	LVDS	1500	Yes
AD9480	1	3.3	1	3.3	LVDS	439	No
AD9481	1	3.3	1	3.3	LVDS	590	No
AT84AS003	2	−5, 3.3	3	−2.2, 2.5, 3.3	LVDS	6500	No
AT84AD004	1	3.3	2	2.25, 3.3	LVDS	1400	Other
AT84AD001	1	3.3	2	2.25, 3.3	LVDS	1400	Other

AT84AS001	1	5	1	3.3	LVDS	2400	Yes
AT84AS004	2	−5, 3.3	3	−2.2, 2.5, 3.3	LVDS	6500	No
TS83102G0	2	−5, 5	2	−5, 1.45	LVDS,ECL	5000	No
EV8AQ160	1	3.3	2	1.8, 1.8	LVDS	3900	Yes
TS83102G0BMGS	2	−5, 5	2	−5, 1.45	LVDS,ECL	5000	No
AT84AS008	2	−5, 5	2	−5 to −2.2, 1.5	LVDS,ECL	5000	No
LTC2241−10	1	2.5	1	2.5	LVDS,CMOS	710	No
LTC2241−12	1	2.5	1	2.5	LVDS,CMOS	710	No
LTC2242−10	1	2.5	1	2.5	LVDS,CMOS	858	No
LTC2242−12	1	2.5	1	2.5	LVDS,CMOS	858	No
MAX104	3	−5, 5, 5	2	3−5, 5	LVPECL	5250	No
MAX106	3	−5, 5, 5	2	3−5, 5	LVPECL	5250	No
MAX108	3	−5, 5, 5	2	3−5, 5	LVPECL	5250	No
MAX1121	1	1.8	1	1.8	LVDS	477	No
MAX1123	1	1.8	1	1.8	LVDS	820	No
MAX1124	1	1.8	1	1.8	LVDS	477	No
MAX1214	1	1.8	1	1.8	LVDS	460	No
MAX1214N	1	1.8	1	1.8	LVDS	799	No
MAX1215	1	1.8	1	1.8	LVDS	1006	No
MAX1215N	1	1.8	1	1.8	LVDS	886	No
MAX1219	1	1.8	1	1.8	LVDS	1600	No
ADC08200	1	3	1	2.4−Vcc	CMOS	210	No
ADC08B200	1	3.3	1	3.3	CMOS	543	No
ADS5440	1	5	1	3.3	LVDS	2250	No
ADS5440−EP	1	5	1	3.3	LVDS	2250	No
ADS5444	1	5	1	3.3	LVDS	2250	No
ADS5444−EP	1	5	1	3.3	LVDS	2250	No
ADS5463	1	5	1	3.3	LVDS	2250	No
ADS5474	1	5	1	3.3	LVDS	2500	No
ADS5527	1	3.3	1	3.3	LVDS,CMOS	1230	No
ADS5547	1	3.3	1	3.3	LVDS,CMOS	1375	No

Table 4: Interfacing Information − Clock

Model	2−Way Demultiplexed Output	Recommended Clock Level V_{pk-pk}	Differential Clock Input	Sinusoidal Clock Input	Duty Cycle Stabilizer
AD12401	No	0.4	Yes	Yes	No
AD9054A−200	Yes	0.8	Yes	No	No
AD9211−200	No	0.2	Yes	No	Yes
AD9211−250	No	0.2	Yes	No	Yes
AD9211−300	No	0.2	Yes	No	Yes
AD9230−210	No	0.2	Yes	No	Yes
AD9230−250	No	0.2	Yes	No	Yes

AD9410	Yes	0.4	Yes	No	No
AD9430−210	Yes	0.2	Yes	No	Yes
AD9480	No	0.2	Yes	No	Yes
AD9481	Yes	0.2	Yes	No	Yes
AT84AS003	Yes	0.452	Yes	No	No
AT84AD004	Yes	0.6	Yes	No	No
AT84AD001	Yes	0.6	Yes	No	No
AT84AS001	No	0.64	Yes	No	No
AT84AS004	Yes	0.452	Yes	Yes	No
TS83102G0	No	0.452	Yes	Yes	No
EV8AQ160	Yes	N/A	N/A	Yes	No
TS83102G0BMGS	No	0.452	Yes	Yes	No
AT84AS008	No	0.452	Yes	Yes	No
LTC2241−10	Yes	0.2	Yes	Yes	Yes
LTC2241−12	Yes	0.2	Yes	Yes	Yes
LTC2242−10	Yes	0.2	Yes	Yes	Yes
LTC2242−12	Yes	0.2	Yes	Yes	Yes
MAX104	Yes	3	Yes	Yes	No
MAX106	Yes	3	Yes	Yes	No
MAX108	Yes	3	Yes	Yes	No
MAX1121	No	0.5	Yes	Yes	Yes (Required)
MAX1123	No	0.5	Yes	Yes	Yes (Required)
MAX1124	No	0.5	Yes	Yes	Yes (Required)
MAX1214	No	0.5	Yes	Yes	Yes (Required)
MAX1214N	No	0.5	Yes	Yes	Yes (Required)
MAX1215	No	0.5	Yes	Yes	Yes (Required)
MAX1215N	No	0.5	Yes	Yes	Yes (Required)
MAX1219	No	0.5	Yes	Yes	Yes (Required)
ADC08200	No	1.2	No	No	No
ADC08B200	No	N/A	No	No	No
ADS5440	No	3	Yes	Yes	No
ADS5440−EP	No	3	Yes	Yes	No
ADS5444	No	3	Yes	Yes	No
ADS5444−EP	No	3	Yes	Yes	No
ADS5463	No	3	Yes	Yes	No
ADS5474	No	3	Yes	Yes	No
ADS5527	No	0.7	Yes	Yes	No
ADS5547	No	0.7	Yes	Yes	No

Table 5: Dynamic Performance Characteristics

Model	$F_{S,Max}$	$Input_{dBFS}$	$SNR_{dB,20MHz}$	$SNR_{dB,80MHz}$	$SFDR_{dBc,20MHz}$	$SFDR_{dBc,80MHz}$
AD12401	400	−1.00	62.93	62.39	84.34	77.93
AD9054A−200	200	−1.00	46.50	46.00	N/A	N/A
AD9211−200	200	−1.00	59.46	59.28	83.50	76.50
AD9211−250	250	−1.00	59.39	59.24	85.00	79.50
AD9211−300	300	−1.00	59.20	59.01	80.00	80.00
AD9230−210	210	−1.00	64.67	63.90	82.50	78.00
AD9230−250	250	−1.00	64.59	64.14	81.00	78.00
AD9410	210	−0.50	54.86	54.05	60.96	59.75
AD9430−210	210	−0.50	65.03	64.04	80.50	82.00
AD9480	250	−1.00	47.14	46.71	69.00	68.00
AD9481	250	−1.00	46.00	45.64	62.50	63.00
AT84AS003	1500	−1.00	53.00	52.80	57.00	57.00
AT84AD004	500	−1.00	46.10	46.20	57.00	56.70
AT84AD001	1000	−1.00	45.00	44.40	58.00	57.00
AT84AS001	500	−1.00	63.02	62.49	75.50	75.30
AT84AS004	2000	−1.00	52.32	52.25	58.00	56.00
TS83102G0	2000	−1.00	50.45	50.22	61.00	61.00
EV8AQ160	5000	N/A	N/A	N/A	N/A	N/A
TS83102G0BMGS	500	−1.00	50.45	50.22	61.00	61.00
AT84AS008	2200	−1.00	53.61	53.44	57.93	57.85
LTC2241−10	210	−1.00	60.57	60.53	76.50	75.08
LTC2241−12	210	−1.00	65.49	65.42	76.50	75.08
LTC2242−10	250	−1.00	60.57	60.53	77.50	74.80
LTC2242−12	250	−1.00	65.57	65.43	77.50	74.80
MAX104	1000	−1.00	47.40	47.00	70.00	69.00
MAX106	600	−1.00	47.50	47.42	73.50	73.00
MAX108	1500	−1.00	48.06	47.94	61.00	61.00
MAX1121	250	−0.50	48.86	48.84	71.00	69.00
MAX1123	210	−0.50	57.43	57.25	77.00	71.50
MAX1124	250	−0.50	57.00	56.80	72.00	71.00
MAX1214	210	−1.00	65.95	65.71	80.00	72.00
MAX1214N	210	−1.00	67.42	66.78	85.00	80.00
MAX1215	250	−1.00	65.92	65.71	82.50	73.00
MAX1215N	250	−1.00	67.04	66.69	85.50	85.00
MAX1219	210	−1.00	67.10	66.59	87.00	82.50
ADC08200	200	−0.25	46.00	44.71	59.33	56.15
ADC08B200	200	−0.25	46.81	45.88	56.30	51.94
ADS5440	210	−1.00	69.93	69.23	81.21	78.55
ADS5440−EP	210	−1.00	69.93	69.23	81.21	78.55
ADS5444	250	−1.00	69.47	68.95	82.06	79.41
ADS5444−EP	250	−1.00	69.47	68.95	82.06	79.41
ADS5463	500	−1.00	64.48	64.34	84.94	83.06
ADS5474	400	−1.00	69.73	69.38	88.08	85.48
ADS5527	210	−1.00	69.70	69.39	84.88	82.26
ADS5547	210	−1.00	72.60	72.02	85.59	82.82

Table Footnotes

The following subsections document notable facts relevant to the tables shown above. In general, these notes do not appreciably supersede the data captured in the table, nor do they alter the outcome of the analysis, but are provided here for completeness.

Top Sheet SNR Audit

At 20 and 80 MHz, all ADCs matched their typical performance characteristics (as seen in Table 5) to within ± 3 dB of the advertised or "top sheet" rating given for SNR on their respective product pages. Of the 45 ADCs, 3 had no advertised SNR data aside from what was contained within their datasheet tables. The advertised SNRs of the remaining 42 were usually derived from input frequency values F_{in} > 20 MHz and tended to be lower than those observed at 20 MHz. At 20 MHz, 33 of the 42 had higher SNR ratings at 20 MHz than the advertised rating, and 38 were within ± 1.50 dB of the advertised SNR. At 80 MHz, 23 (just over half) had higher SNR ratings than the advertised value and 39 were within ± 1.50 dB of the advertised SNR.

Input Clock Requirements

The encode clock is a very important part of high−speed ADC system design. Interestingly, older ADCs appear to have less stringent clock requirements, as dictated by minimum acceptable duty cycle. All ADCs studied can function with a duty cycle that varies from 45−55%, although many can accept larger variations in duty cycle. Approximately half of the ADCs reviewed contain internal clock duty cycle stabilizer circuits. ADCs which contain *optional* stabilizer circuits allow for greater tolerances in duty cycle variation than are listed in Table 4. For all others, including Maxim ADCs where stabilizer circuits cannot be disabled, the values listed in the table are accurate.

Minimum sampling frequencies $F_{S,Min}$ were all derived from datasheet tables, but minimum duty cycles came from a variety of sources within the datasheets: direct expression in tables, literature describing clock input requirements, by relating minimum clock high time to the length of clock period at max sampling frequency $F_{S,Max}$, and occasionally by finding practical roll−off points in charts that compare SNR or SFDR vs. clock duty cycle. The "Duty, Clock" sheet within the attached spreadsheet shows corresponding notes for cases in which the minimum duty cycles were read from graphs or inferred from clock high time and clock period.

There is surprisingly little information listed in the datasheets specifying clock slew rate requirements for the devices that require square edges. For sinusoidal input clocks, large clock amplitudes were recommended to maximize slew rate.

Dynamic Performance Characteristics

Please note that not all dynamic performance characteristics shown in Table 5 are called out numerically in the datasheets. However, for the purposes of this study, the SNR_{dB} vs. frequency graphs are smooth enough to make an approximation given a few data points. SFDR was a bit less straightforward, since it is often irregular in the range of interest. Therefore, for many candidates, points on charts were selected when linear approximation did not seem reasonable. For more detail on how items of interest were calculated, please see the attached spreadsheet , in which the 'Master' sheet references sheets 'SNR' and 'SFDR'. The actual calculations are given on the latter sheets.

Detailed Architecture Information

More−detailed information on each ADC's architecture is not generally available. We called Analog Devices, Maxim, and Linear on 7/2/07 to obtain more information on the number of stages in their ADC architectures and the number of bits encoded per stage.

The engineer at Analog would not give us specific information after not finding any on the datasheet himself. He instead mentioned that the ADCs were designed for continuous operation, and that once the first latency period had elapsed, the data stream from the output would simply be a time−shifted version of what was coming out of the input. Therefore, the internal architecture shouldn't be of much concern to us. He recommended we call back when we had "narrowed down our selection to two, or maybe three ADCs... [and could] give more information on the application" and why we would need the architecture information. From there, he said, maybe we would be able to talk to some of the design engineers responsible for the chips to elaborate further. He suggested we use the web−based design tool ADIsimADC or the related standalone software to evaluate their converters' capabilities to figure out how the parts might best be applied in our situation.

The engineer with whom we spoke at Maxim, Hubert, first surmised the 2 bits per stage might not include error checking bits, or else the number of stages would be easy to determine (1 bit for EC would leave only 1 useful bit per stage of conversion, giving exactly as many pipeline stages as the ADC's resolution). We told him we were asking about the Maxim chips in the 112x line. He called us back after checking on this, and said that his manager told him not to give us the information on number of stages as it was proprietary, and furthermore told Hubert not to look it up himself (presumably to prevent intentional or accidental disclosure). He closed by saying that the pipeline latency in terms of cycles might give hints as to pipeline length.

The correspondent at Linear, Allison, returned our call on 7/3/07 and left a message stating that their pipeline architecture information was also proprietary information and that they would like more application information to understand how our designs might be impacted by the internal workings of the ADC.

Date of First Availability

Although we attempted to obtain the data of first availability for each candidate ADC, most vendors were reluctant or seemingly unable to provide this data. At least one vendor referred us to the course granularity ("announced", "in production", "mature", "lifetime buy", or "discontinued") life−cycle information as the only available relevant data. While we have captured the data we have managed to obtain thus far, we have an ongoing telephone/email effort for the purpose of obtaining this information. It seems primarily to be a process of repeated contact until we find a person willing to disclose the data.

Down Selection

After the thorough market survey documented above, we were pleasantly surprised to find that there are at least 45 viable ADC candidates for the Long Wavelength Array. The following selection documents the process of narrowing this rather large field for the purpose of selecting 3−6 candidates for further evaluation.

Outlier Removal

Mindful of the large number of candidates, we then developed four objective criteria to remove obvious outliers and narrow the field:

1. ADCs whose datasheets have not been updated since 12/03 were removed from further consideration. These ADCs are typically older, and are believed to have a greater probability of being discontinued.
2. ADCs priced at greater than $150 per unit (in volumes of 1000) were eliminated.
3. ADCs contained in a BGA (ball−grid array) or CGA (ceramic ball grid array) were eliminated. The possibility of rework during the prototyping phases is a daunting task at best, and the proper equipment to do so with BGA chips is expensive and is best avoided if possible.
4. ADCs requiring 3 or more power supplies were eliminated. The need for clean supplies in a high−speed converter is paramount to ensuring signal quality, and therefore each supply must be properly decoupled and filtered. Separate digital and analog supplies are certainly needed, but having more than one of each can unnecessarily complicate the design.

In all, 15 candidates were eliminated from consideration using these four criteria, leaving 30 candidates for further study.

Pareto−dominated Candidate Removal

A Pareto dominatation analysis was then performed on the remaining candidates using seven metrics: 1) price, 2) power, 3) SNR at 20 MHz, 4) SNR at 80 MHz, 5) SFDR at 20 MHz, 6) SFDR at 80 MHz, and 7) maximum sample rate. In this analysis, candidates are removed from consideration in which there exists another candidate that ranks higher on all seven metrics. In traditional Pareto terminology, such candidates are referred to as being "dominated", and represent a suboptimal selection that can be safely removed from consideration.

Table 6 summarizes the 23 eliminated ADCs from the initial set of 45. The relevant elimination criteria and relevant values are enumerated in their respective columns.

Table 6: Elimination Results

Model	Latest Rev	Cost	Packaging	Power Supply	Pareto−Dominated By
AD9054A−200	May−01				
MAX108	Oct−01	$350.00	ESBGA	5	
MAX106	Nov−01		ESBGA	5	
MAX104	Mar−02	$199.00	ESBGA	5	
AT84AD001		$178.00		3	
AD12401		$525.00		3	
TS83102G0		$1,263.00	CBGA	4	
AT84AS008		$1,390.00	CI−CGA, CBGA	4	
TS83102G0BMGS			CI−CGA	4	
AT84AS003			EBGA	5	
AT84AS001			EBGA		
AT84AS004			EBGA	5	
EV8AQ160			EBGA	3	
AD9410				3	
AD9430−210					ADS5527
AD9481					AD9480
AT84AD004				3	
MAX1123					LTC2241−10
MAX1124					AD9211−250
MAX1215					MAX1215N
ADC08B200					AD9480
ADS5440−EP					ADS5440, ADS5527
ADS5444−EP					ADS5444

Pareto Analysis

Further down selection from these 22 ADCs is accomplished by Pareto analysis over four metrics:

- Typical power dissipation (mW)
- The minimum of SNR observed at input frequencies of 20 MHz and 80 MHz (dB)

- The minimum of SFDR observed at input frequencies of 20 MHz and 80 MHz (dBc)
- Price per input channel ($)

The maximum sample rate (MSPS) of the ADCs was included in this analysis, although it is handled differently from the other four metrics. Based upon the findings from earlier sections, it is likely that the sample rate selected for LWA will be one of three values:

1. 200 MSPS which is the minimum feasible value,
2. 250 MSPS which is the sample rate above which the majority of ADCs under study are not qualified to operate, or
3. 256 MSPS which provides integer divisors and ample margin for anti−alias rolloff.

As a result, in the remaining analysis and associated graphics we explicitly consider three Pareto frontiers for each of the three sample rate values shown above.

Out of the pairwise combinations of the four key metrics listed above, two were found to possess poor Pareto frontiers: 1) SFDR vs. SNR, and 2) Price per channel vs. Power. Often poor pareto frontiers are associated with a (perhaps unmodeled) dependent relationship between the metrics in question, and can indicate that there exists little trade−off to be made between the metrics.

Such a dependent relationship appears in Figure 2, which plots minimum SFDR against minimum SNR. In this case, improved device linearity and dynamic range impacts both SNR and SFDR, as one might expect.

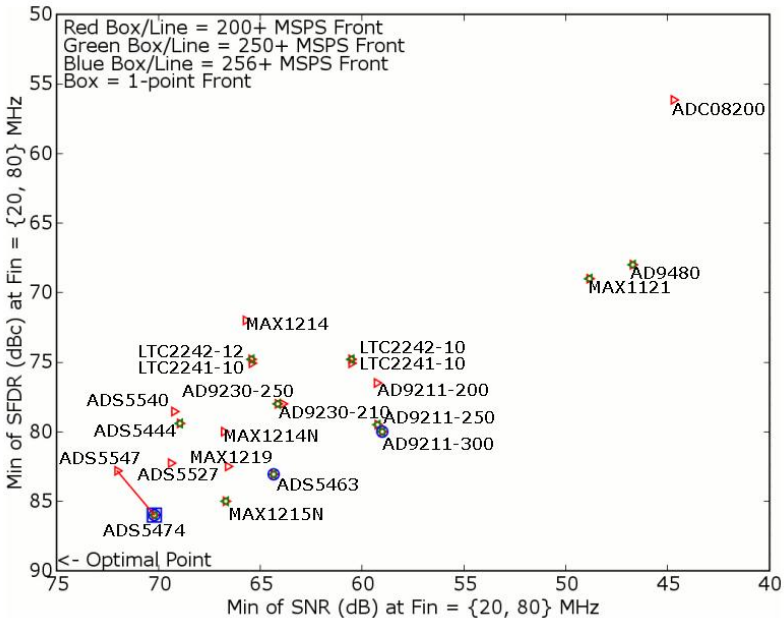

Figure 2: Pareto Analysis: SFDR vs. SNR

The comparison of typical power dissipation plotted against price per channel shown in Figure 3 reveals a similarly poor Pareto front. In general, selecting for lower powered devices also means simultaneous selection for lower priced devices. Although it is difficult to state a direct causal relationship, higher power dissipation often implies more expensive packaging and poorer yields, which might explain a portion of this effect.

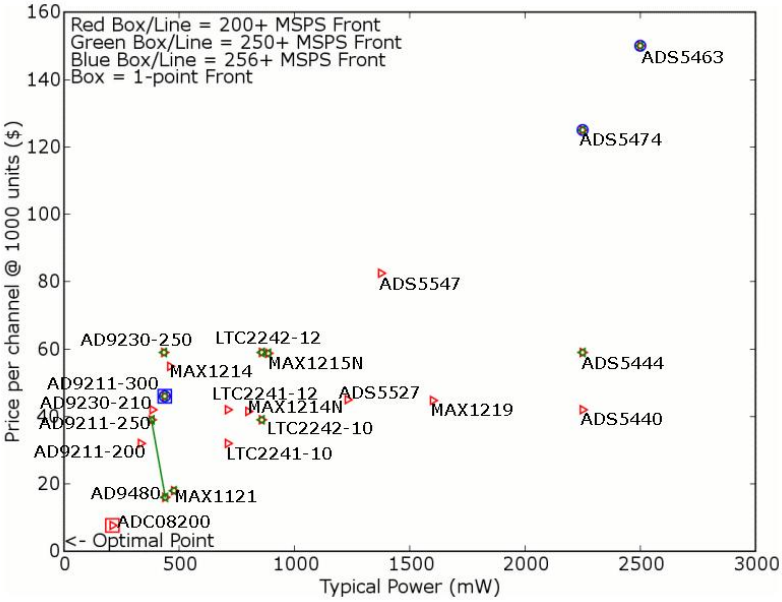

Figure 3: Pareto Analysis: Price per channel vs. Power

Given the two dependent relationships described, it is only necessary to consider four remaining pairwise combinations of the four chosen metrics. These are shown in Figures 4, 5, 6, and 7.

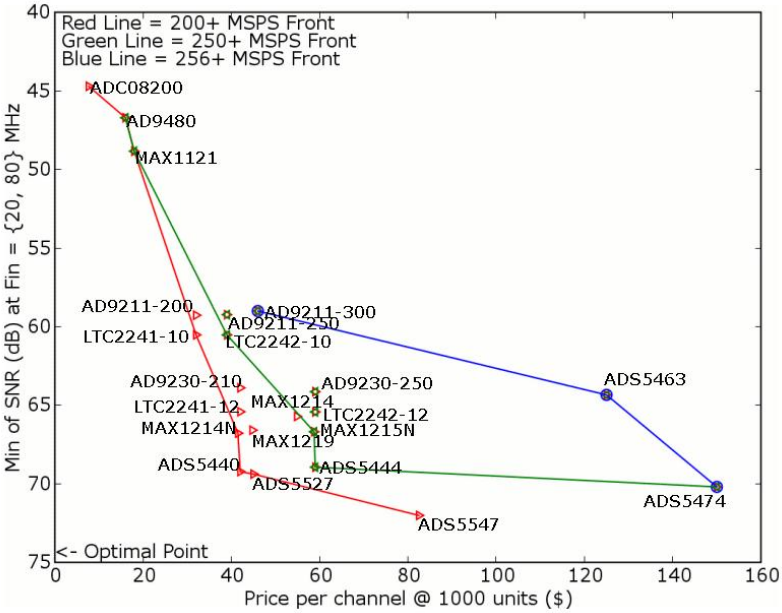

Figure 4: Pareto Analysis: SNR vs. Price per channel

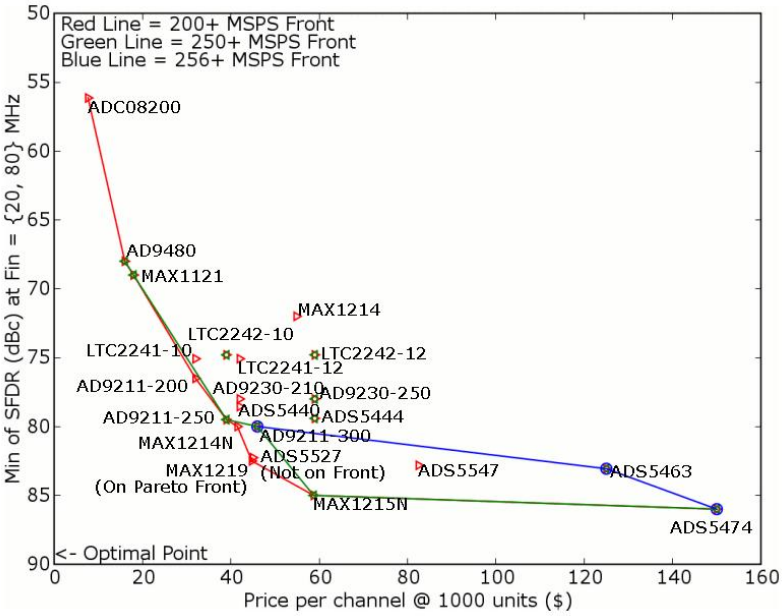

Figure 5: Pareto Analysis: SFDR vs. Price per channel

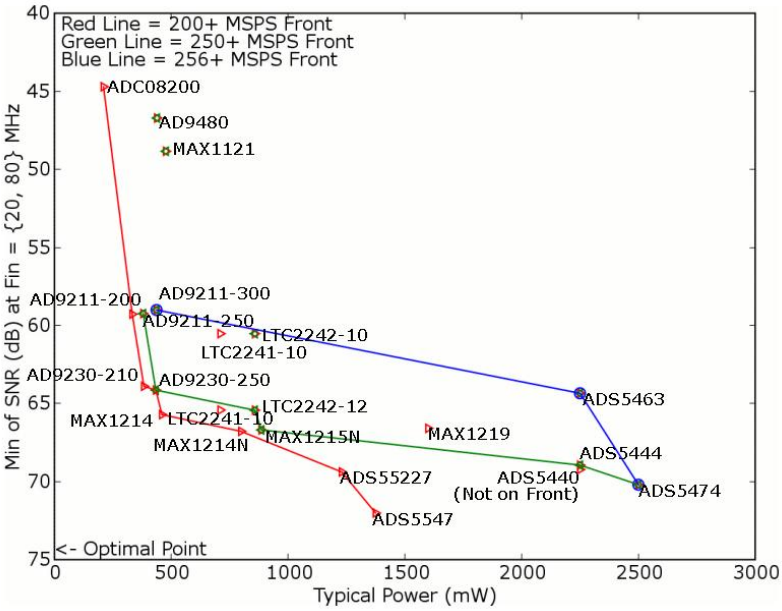

Figure 6: Pareto Analysis: SNR vs. Power

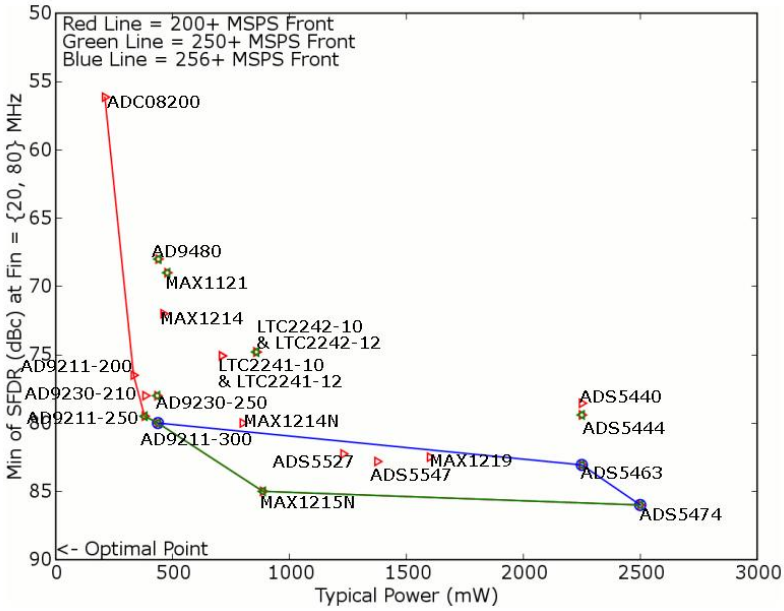

Figure 7: Pareto Analysis: SFDR vs. Power

Candidate Selection Strategy

In the context of the Parteo analysis detailed above, without further assumptions there are at least three obvious strategies for picking candidates for further evaluation:

1. Pick candidates that are optimal in one of the metrics (the flank of the Pareto frontier),
2. Pick candidates that tend to be optimal in all regards (the knee of the Pareto frontier curve), or
3. Pick candidates that span the Pareto optimal frontier (that are spaced out across the entire Pareto frontier).

The first strategy is preferable when there is a single metric that is known to be more critical than the others for the intended application. The second strategy is preferable when little is known about the relative priorities of the various metrics, and it is expected that no further information will be gained. The third strategy has risk−mitigation benefits, and is preferable when little is known about the relative priorities of the various metrics, but it is expected that such information may become available at a later date or through further testing.

For LWA, which is clearly constrained in non−obvious ways by cost, power, and performance, but for which there is no obviously dominating metric as of yet, it is the recommendation of the authors that the candidates be selected that are spaced out across the Pareto optimal frontier. It should be noted that at this point in the development process, there is no expectation that any of the ADCs listed here will perform unsuitably for LWA. That is, we have every reason to believe that each of these ADCs will perform adequately, and the present question is simply to pick the best of the field based upon incomplete information. By picking candidates that span the frontier, we hedge our bets, and increase the probability of success in the event that future development shows the disproportionate criticality of a particular metric: cost, power, or performance

ADC Candidates for Further Evaluation

In the preceding section, a rationale was given for selecting ADCs that span the Pareto frontier for further evaluation. In order to do this in an objective manner, we have developed a number of objective ranking methods, and discovered that six ADCs appear frequently near the top of these rankings. The results of one such method is detailed below.

The values in Table 7 indicate the number of times each ADC appears on the Pareto frontier of the graphs shown in Figures 4, 5, 6, and 7.

Table 7: 22 ADCs: Pareto Frontier Appearance Rate in Figures 4−7

Model	MSPS	200+	250+	256+
AD9211−200	200	3	−	−
AD9211−250	250	2	3	−
AD9211−300	300	1	2	4
AD9230−210	210	1	−	−
AD9230−250	250	1	1	−
AD9480	250	2	2	−
LTC2241−10	210	1	−	−
LTC2241−12	210	0	−	−
LTC2242−10	250	0	1	−
LTC2242−12	250	0	1	−
MAX1121	250	2	2	−
MAX1214	210	1	−	−
MAX1214N	210	3	−	−
MAX1215N	250	2	4	−
MAX1219	210	1	−	−
ADC08200	200	4	−	−
ADS5440	210	1	−	−
ADS5444	250	0	2	−
ADS5463	500	0	0	4
ADS5474	400	2	4	4
ADS5527	210	2	−	−
ADS5547	210	2	−	−

In Table 7, five ADCs stand out as being Pareto optimal four times (out of four) at a given sampling rate: AD9211−300, MAX1215N, ADC08200, ADS5463, ADS5474. In addition, in the course of contacting vendors for the purpose of obtaining information for this document, an evaluation board for the Linear technology LTC2241−10 has been made available at no cost. Examination of Figures 4, 5, 6, and 7 shows that these six ADCs roughly span the Pareto frontiers for various sample rate options.

Moreover, the selection of these six ADC candidates for further study has several desirable characteristics:

- All five manufacturers that make suitable ADCs are represented
- Both components consistently on the extremes of the Pareto frontier are included (ADC08200, and ADS5474)
- Several components reside near the knee of the Patero frontier
- The entire 256+MSPS Pareto frontier is represented
- The datasheets for all six components have been released or revised after April 2006
- Five of the six components are members of larger product lines, and to some degree represent alternative candidates

Conclusion

This document details a comprehensive market survey of 45 analog to digital converter candidates for the Long Wavelength Array (LWA). Through various objective means 15 of these candidates were eliminated

from consideration, leaving 30 viable candidates. A Pareto analysis was undertaken for these candidates, and notable characteristics of the parameter space were documented. Based upon the current state of LWA development, a risk mitigation rationale has been provided for the strategy of choosing candidates that span the Pareto optimal frontier. Using this strategy, a set of six candidate ADCs with desirable properties have been selected for further study. Based upon this analysis, we recommend the further laboratory evaluation of six ADCs: AD9211−300, MAX1215N, ADC08200, ADS5463, ADS5474, and LTC2241−10.