Collected LWA Engineering Memos
From the Development of the Analog Receiver (ARX) Rev. I

2023 August 28 – 2024 October 21

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ARX-Eval-01

Evaluation of the TI TPS16412 eFuse for Use in the Rev. I ARX

28 August 2023

Whitham D. Reeve

Evaluation of the TI TPS16412 eFuse for Use in the Rev. I ARX
Whitham D. Reeve

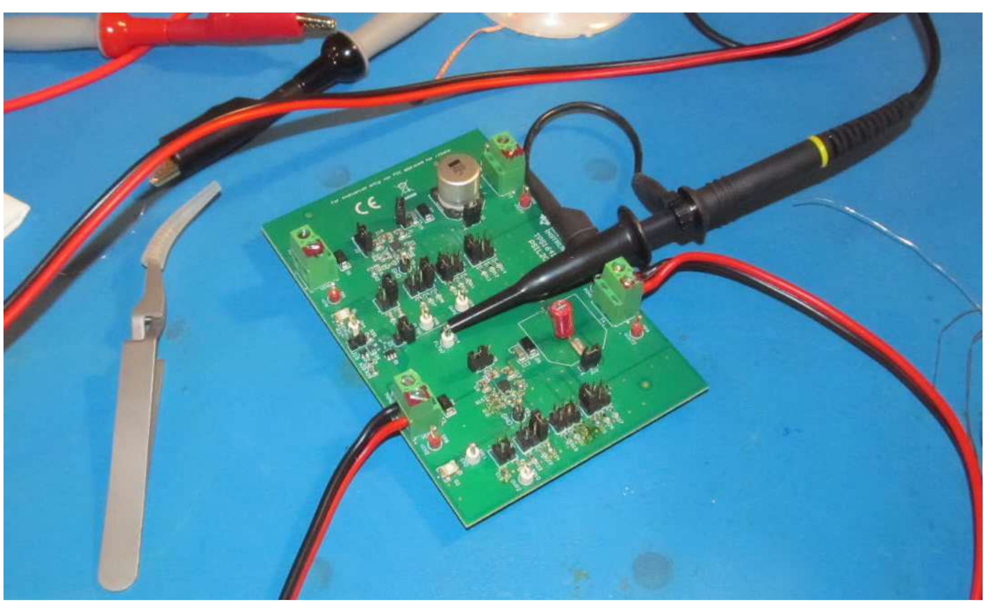
This document describes the evaluation of the TPS16412 eFuse as it applies to the Rev. I ARX design. In this application, the eFuse is used to connect and disconnect power from the Front End Electronics (FEE) while limiting the current to protect the bias-tee components from overcurrent. The eFuse also provides fault indication and load current monitoring.

The evaluation included the following functions and associated device pins:

- ✓ Enable and shutdown control (EN/SHDN)
- ✓ Overvoltage protection (OVP)
- ✓ Voltage slew rate (dV/dt)
- ✓ Current limiting (ILIM)
- ✓ Blanking time delay (IDLY)
- ✓ Overcurrent protection (IOCP/IMON)
- ✓ Fault (FLT)

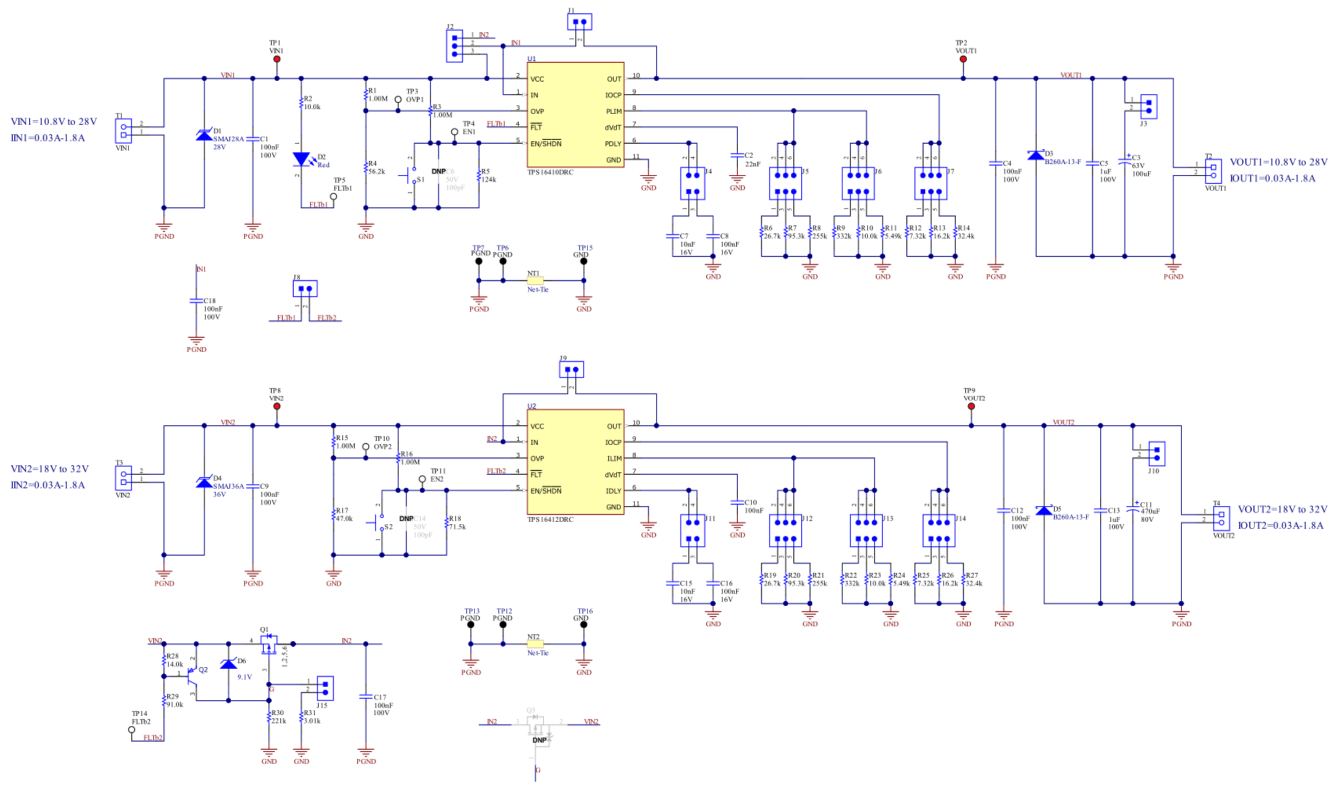
The evaluation was primarily designed to determine if the output voltage slew rate could be reduced to provide a ramp from 0 to 15 V in 100 ms to protect the output stage of the V1.8 Front End Electronics from transients. The TPS16412 datasheet does not directly address the possible internal heating effects of such a long voltage ramp, but the device design clearly supports a large range of slew rates. The concern was that the eFuse inherent overtemperature protection may trip the device before it reached full operating voltage. All functions, including the voltage slew rate, were found to work as designed.

Evaluation module: Evaluation of the device was simplified by the Texas Instruments TPS1641EVM evaluation module shown in the image below. The EVM has two channels. Channel 1 uses the TPS16410 eFuse for power limited evaluation; and Channel 2 uses the TPS16412 eFuse for current limited evaluation; only the TPS16412 is evaluated here.



Modified TPS1641EVM evaluation module. See text for modifications. The channel evaluated is on the lower-right. An oscilloscope probe is connected to a test point. Power supply and load connections are through terminal blocks. Component values for different operating conditions are selected by jumper blocks along the lower-right side.

The evaluation module provides terminal blocks for input power and output load connections and uses headers and jumpers to set the evaluation parameters through on-board capacitors and resistors. Several of the component values on the stock evaluation board were not compatible with the Rev. I ARX receiver application so they were replaced. The EVM also includes input and output transient voltage protection components, which were left in-place. See schematic below.



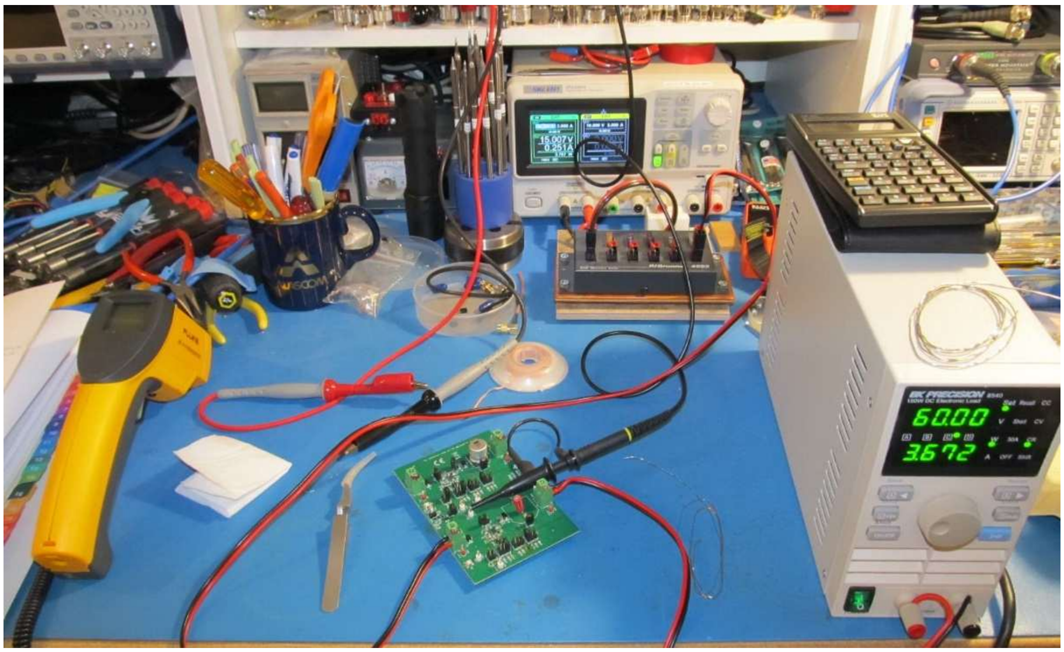
TPS1641EVM schematic. The lower channel has the TPS16412 and is the only one evaluated. Some components and connections are shared between the two channels, so both are shown.

<u>Test equipment</u>: Siglent SPD3303X 3-channel variable power supply, Keithley 2110 bench DMM, BK Precision 8540 Electronic Load, Siglent SDS2302X 2-channel oscilloscope, Fluke 63 IR Thermometer, Hakko FR-830 PCB Preheater.

<u>Initial tests</u>: The EVM was first checked for general operation with its default components and settings for 18-32 Vdc input and 1 A current limit (30 mA, and 1 and 1.8 A current limit settings are available). Overcurrent protection was set to 1.01 A (0.5, 1.01 and 2.23 A overcurrent settings are available).

The electronic load was set to the Constant Resistance mode and the resistance adjusted to provide the desired load current. For the initial tests, the resistance was set to 36 ohms to provide a load of 0.5 A at 18 V. The resistance was then reduced in 1 ohm increments to 18 ohms to increase the current to the current limit of 1 A at 18 V. The load resistance was further decreased to 17.8 ohms to trip the overcurrent protection. The voltage slew rate was checked with the default capacitor CdVdt (C10 = 100 nF) and blanking time based on default capacitors (C15 or C16).

ARX application tests: For all application tests specific to the ARX described below, the EVM was connected to the variable power supply and electronic load through 18 AWG cables. The power supply output voltage was set to 15.0 V except for the overvoltage protection tests. The power supply output current limit was set to 2.0 A for all tests. The electronic load was set to constant resistance mode and varied as needed. Device temperature was monitored with a Fluke 63 IR Thermometer held about 25 mm from the device package on the PCB. The basic setup is shown in the image below. Refer to ***TPS16412 eFuse Application*** for specific design methodologies and details for the ARX application [See References at the end].



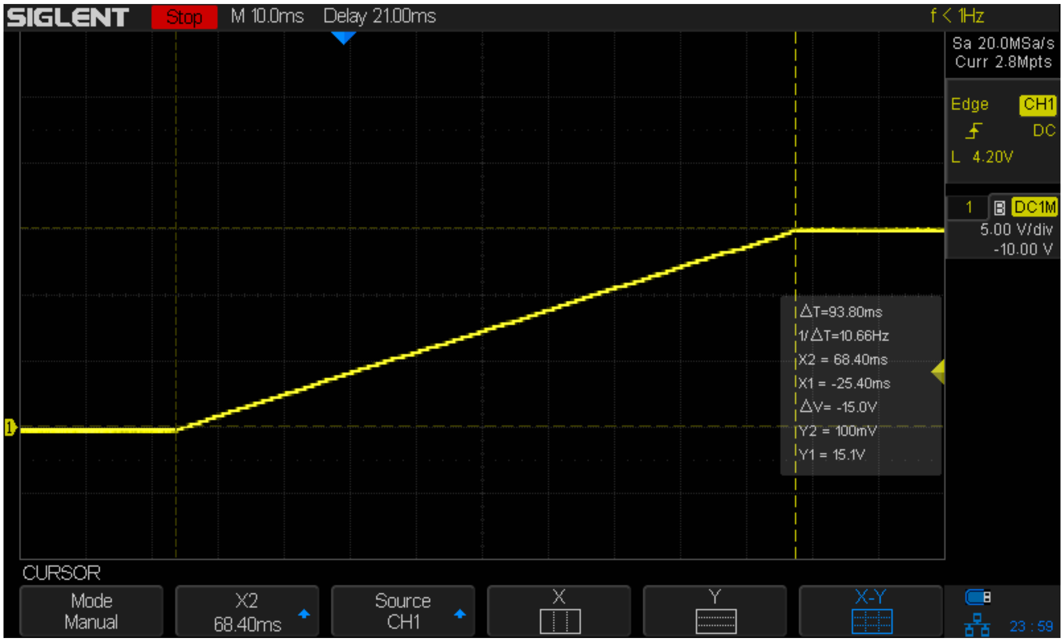
EVM test setup showing the variable power supply in the background, electronic load in the right-foreground and EVM in the middle-foreground. The electronic load is set to the constant resistance mode. The oscilloscope and DMM are outside the view. The IR thermometer is on the left.

Enable and shutdown control (EN/SHDN): The TPS16412 on the EVM is enabled by a 1 Mohm pullup resistor connected to the device operating voltage pin Vcc. The EVM has a pushbutton that shorts the pin to ground to shutdown the device. This function worked as expected.

Overvoltage protection (OVP): The OVP function on the EVM was originally set to 33 V through a resistive voltage divider R15 (1 Mohm) and R17 (47.0 kohm). Resistor R15 was left as original and R17 was replaced with a 68.1 kohm resistor to lower the voltage to about 23.5 V. With the new resistor, the input voltage was raised from 15.0 V until the unit tripped at the new voltage. When tripped, the internal FET is disabled, which removes voltage from the device output, and the fault pin is pulled low.

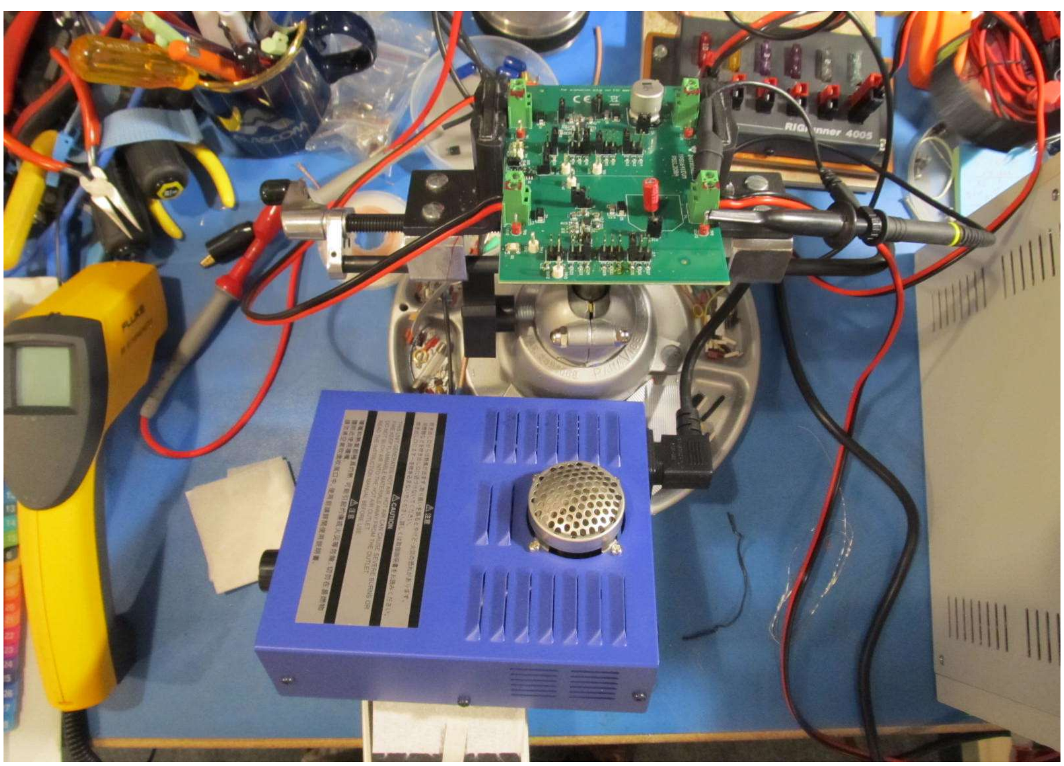
Voltage slew rate (dVdt): The output voltage slew rate and inrush current are related. The inrush current is controlled by the load capacitance on the device. The EVM originally was equipped with a fixed 1 µF capacitor (C13) and a jumper selectable 470 µF capacitor on its output (C11). Capacitor C11 was removed and replaced with a 10 µF capacitor to control the inrush current equivalent to the ARX design. A separate dVdt capacitor determines the slew rate. The original dVdt capacitor (C10) was 100 nF. It was replaced with a 0.68 µF (±10%) MLCC to provide a design slew rate of 150 V/s. The slew rate of the output voltage was measured with an oscilloscope by placing the X and Y cursors at the 0 and 100% voltage points. The measured time difference was

93.8 ms, giving a slew rate of 159.9 V/s. See the oscilloscope screenshot below. These tests were at room temperature.



Measured voltage ramp at room temperature. Timebase set to 10 ms/div and vertical scale set to 5 V/div with 0 V reference shown by the triangular icon on the left side. The table near the right shows the X and Y cursor settings (only one of the vertical cursors is visible in this image). The ΔT from 0 to 100% of the voltage ramp is 93.8 ms.

A Hakko FR-830 PCB Preheater was then placed to blow hot air on the bottom of the PCB to raise the device temperature; see image below. The minimum setting of the preheater is 150 °C but it was found for the experimental setup that a setting about 160 – 170 °C was adequate to raise the eFuse temperature to 48 °C. The temperature was measured with the IR thermometer by holding it about 25 mm from the device.



Test setup with the PCB preheater. The preheater is at the bottom of the image, and the EVM is held in a Panavise multipurpose vise above the preheater. Both were set at an angle with the preheater air output pointed at the bottom of the EVM. The IR thermometer is the on the far-left.

This test was designed to simulate the higher temperatures in the confined space of the ARX PCB card rack. The device temperature was raised over a period of several minutes while periodically connecting and disconnecting the input voltage to observe the voltage ramp on an oscilloscope. The load current for these measurements was 255 mA to simulate the V1.8 FEE. No failures to start were observed. See the oscilloscope screenshot below.

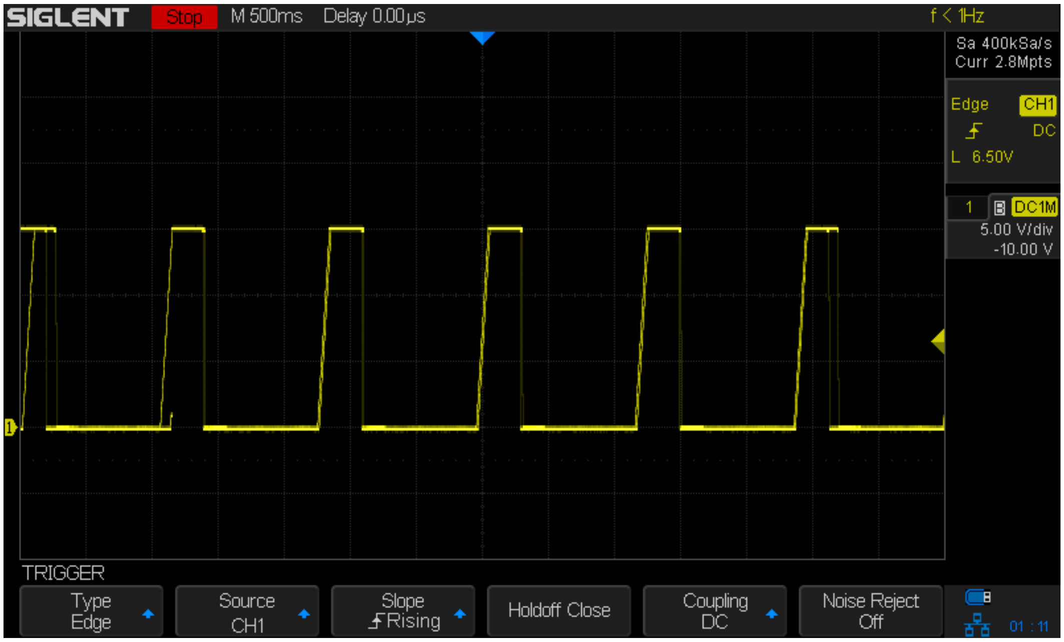
Voltage ramp with device temperature at 48 °C. There was no change in the ramp time and no failures to start over dozens of power cycles. Timebase set to 20 ms/div and vertical scale set to 5 V/div with 0 V reference shown by the triangular icon on the left side.

<u>Current limiting (ILIM)</u>: Current limiting is set by a resistor connected between the ILIM pin and ground. The factory EVM has jumper selectable resistors (J12 and J13) but none of them were near the desired value. The calculated RILIM value for the ARX was 32.8 kohms, but the nearest value available from stock was 35.7 kohms. This resistor was installed and provided a 276 mA current limit. It was noted that both the current limit and overcurrent protection (described below) lead to device tripping caused by high power dissipation in the internal FET junction.

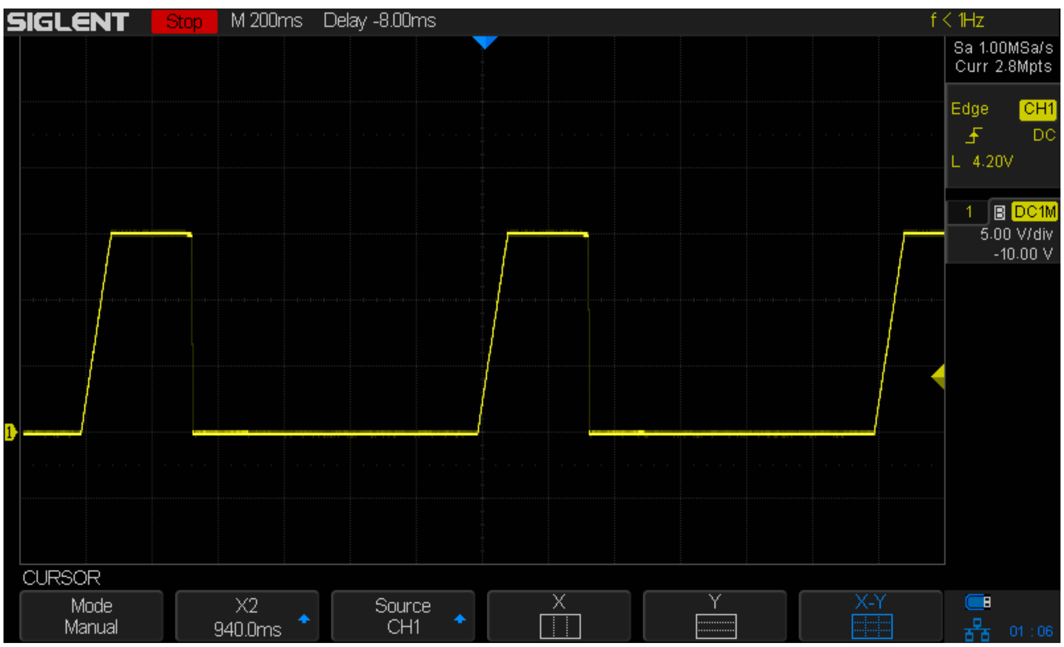
<u>Blanking time (IDLY)</u>: The blanking time was disabled by removing the jumper block on J11 so that the IDLY pin was open-circuited.

<u>Overcurrent protection (IOCP/IMON)</u>: In conjunction with the current limit described above, the device has jumper selectable overcurrent protection resistors (J14) but none were usable. The desired value was 47.0 kohms but a 43.2 kohms resistor was available from stock and installed in place of one of the factory resistors. On rising load current (falling load resistance to 46.5 ohms), the IOCP tripped at 323 mA. There was some hysteresis so the ICOP tripped condition automatically reset when the load current was decreased to 321 mA (increasing the load resistance to 46.8 ohms).

After the device trips due to current limit or overcurrent, it tries to automatically reset (auto-retry). If the overcurrent condition still exists, the TPS16412 will trip again. The TPS16412 does not latch in the tripped state. As long as the overcurrent condition exists, the device will periodically trip and reset as shown in the oscilloscope screenshots below. Note that a similar device, the TPS16413, will latch off rather than auto-retry.



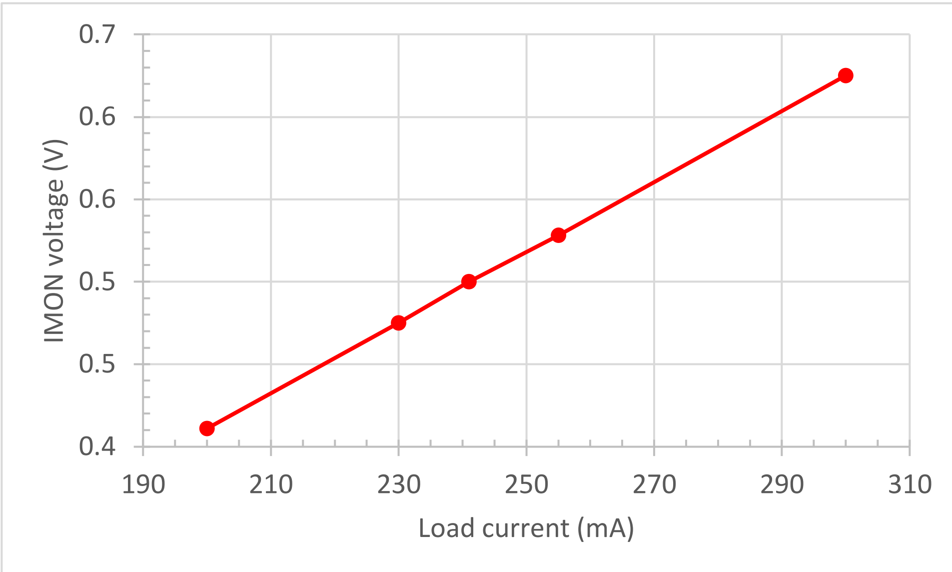
Output voltage with 0.1 ohm short circuit on the output. Note the period is approximately 1.2 s. Timebase set to 500 ms/div and vertical scale set to 5 V/div with 0 V reference shown by the triangular icon on the left side.



Output voltage with 1.67 A current (9.0 ohm load). Note the period is approximately 1.2 s. Timebase is set to 200 ms/div and vertical scale is 5 V/div with 0 V reference shown by the triangular icon on the left side.

<u>Load current monitoring</u>: The voltage at the IOCP/IMON pin can be used to derive the load current. Therefore, the pin was monitored during normal operation with various load currents from 200 to 300 mA. The voltages measured from the IOCP/IMON pin to ground are listed and plotted below. Note the high linearity of the plot.

- 200 mA: 0.411 V
- 230 mA: 0.475 V
- 241 mA: 0.500 V
- 255 mA: 0.528 V
- 300 mA: 0.625 V

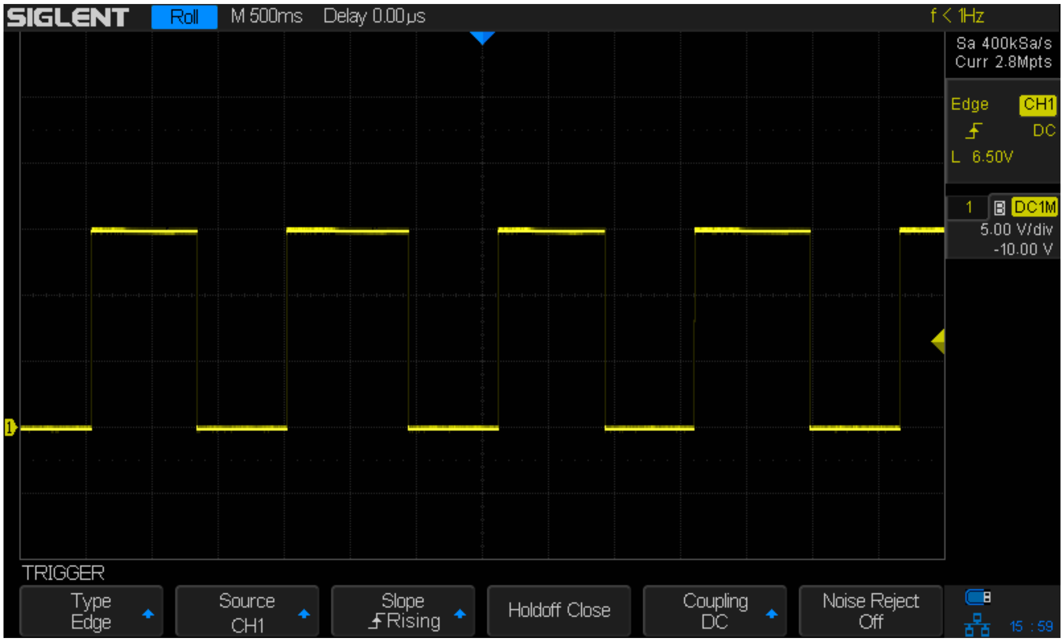


IMON pin voltage for load currents from 200 to 300 mA. The dots indicate the measured values.

Fault (FLT): The various fault conditions in the eFuse are:

- ✓ Overvoltage protection (tested)
- X IN-to-OUT Short detection (not tested)
- ✓ Thermal shutdown (tested)
- ✓ Current limiting timeout (tested)

The Fault pin is pulled low during a fault and pulled high through a pull-up resistor during normal operation. As previously described, the device attempts to automatically reset and does not latch. With a fault continuously applied to the output, the FLT pin pulses between a high and low condition in cadence with the attempts to reset. See the oscilloscope screenshots below for the faulted and normal conditions. The device temperature was measured to see if it would eventually rise due to the cyclic nature of the auto-retry function, but it remained at room temperature overnight, indicating the device protects itself regardless of the auto-retry duty cycle.



Fault pin is periodically pulled low from 15 V to 0 V with 323 mA load current (overcurrent condition). The period is approximately 1.2 s. Timebase is set to 500 ms/div and vertical scale is set to 5 V/div with 0 V reference shown by the triangular icon on the left side.

Fault pin at 250 mA load current (normal condition) is pulled high. The indication is a steady 15 V. Timebase and vertical scale as above with 0 V reference shown by the triangular icon on the left side.

<u>Modifications to factory EVM components</u>: The following components were replaced on the EVM.

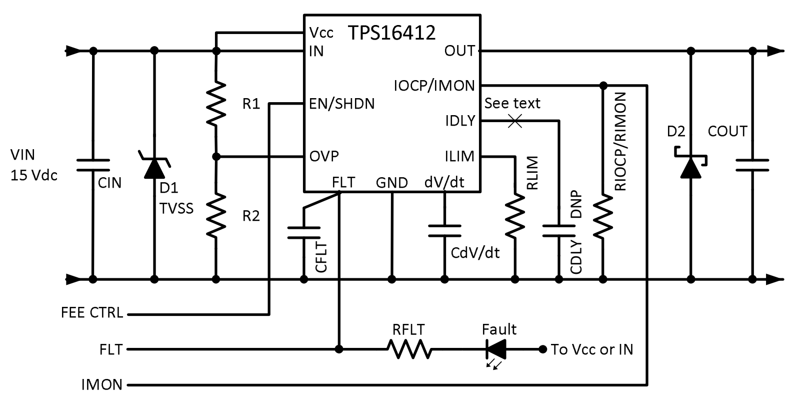
Function	**EVM component designation**	**Calculated modification**	**Size**
IDLY	C15 or C16	CDLY = GND or Open	N/A
dV/dt	C10	CdVdt = 0.68 µF	0603
ILIM	R19, R20, R21 or R22, R23, R24	RLIM = 32.4 kohm	0603
IOCP	R25, R26, R27	RIOCP = 47.5 kohm	0603
OVP	R15 & R17	R1 = 1 Mohm (ok), R2 = 68.1 kohm	0603
COUT	C11 or C13	COUT = 10 µF, 50 V	radial or 1206

EVM settings:

Jumper	Default setting	Default function	New setting	New function
J9	Open	No FET short	Open	No FET short
J10	Shorted	Connect bulk output capacitor COUT = 470 µF	Shorted	Bulk output capacitor COUT = 10 µF
J11	3-4	50 ms blanking time for current limit	Open	No blanking time for current limit
J12	Open	Not used	Open	Not used
J13	5-6	1.8 A current limit	3-4	276 mA current limit
J14	1-2	2.23 A overcurrent protection	3-4	323 mA overcurrent protection
J15	Open	No fast turn-on for Q1 input to channel 2	Open	No fast turn-on for Q1 input to channel 2

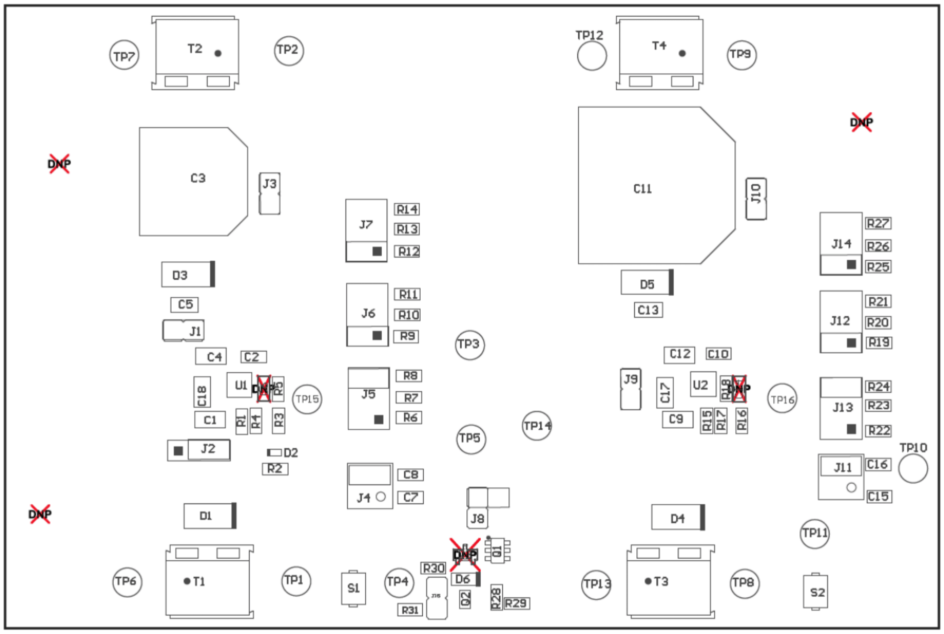
Summary of components in ARX application (see application schematic below):

Component	Value	Remarks	Mfr
R1	1 Mohm, 1%		
R2	68.1 kohm, 1%		
CdVdt	0.68 µF, 50 V, 5%		
RLIM	32.4 kohm, 1%		
RIOCP	47.5 kohm, 1%		
CDLY	Not used (see text)	Connect pin to GND or open	
CFLT	1 nF, 50 V		
D1	18 to 36 V	SMAJ-series	Littelfuse TVS
D2	60 V	B260A or B360A	Diodes, Inc. Schottky
COUT	10 µF + 0.1 µF	Both MLCC, Low ESR	
CIN	1 µF + 0.1 µF	Both MLCC	

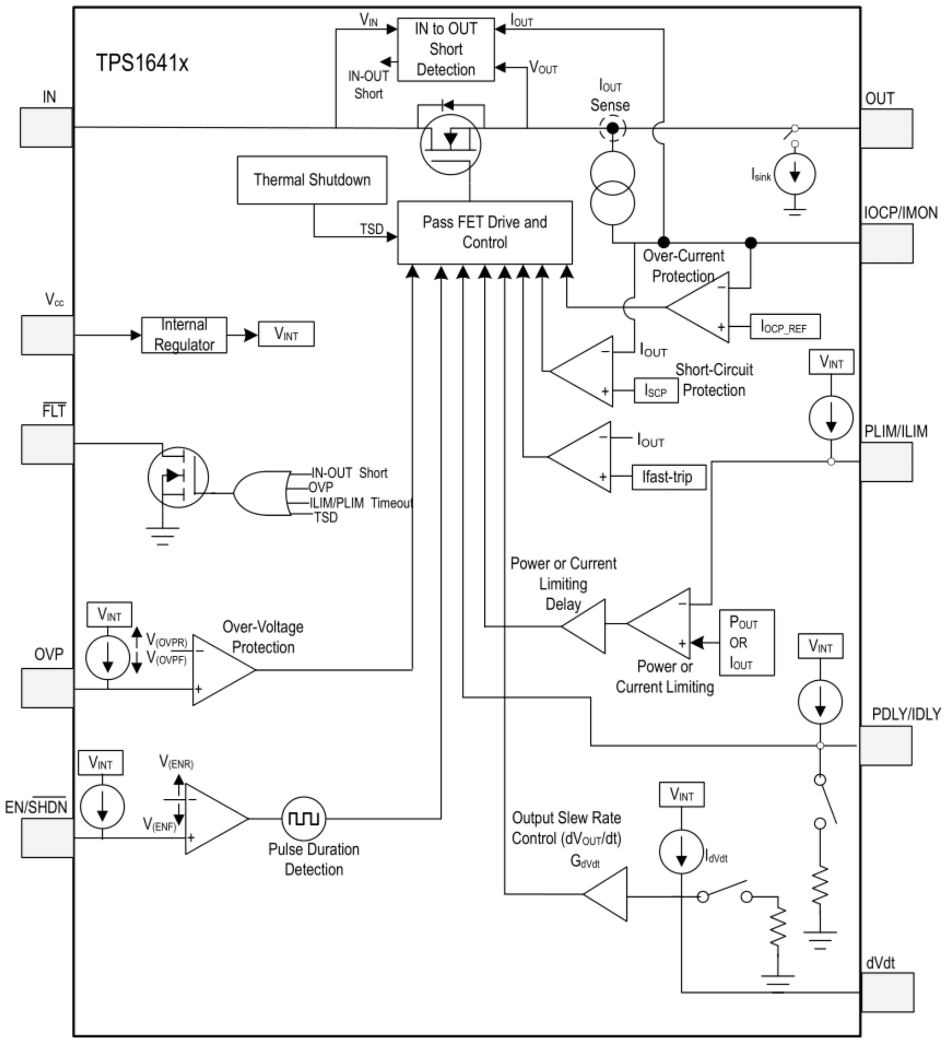


TPS16412 application schematic for the ARX.

<u>TPS16412EVM PCB Layout</u>:



TPS16412 block diagram:



References:
Reeve, W., ***TPS16412 eFuse Application***
Texas Instruments, TPS1641EVM evaluation module

Document Information

Author: Whitham D. Reeve

Revisions: 0.0 (Original draft started, 19 Apr 2023)

0.1 (Added measurements, 22 Apr 2023)

0.2 (Completed 1st draft, 23 Apr 2023)

0.3 (Improved formatting and removed Draft watermark, 28 Aug 2023)

Word count: 2411

File size (bytes): 1387574

Memo Cover Sheet

ARX-Eval-02

Logic & Monitoring Components Evaluation
29 September 2023
Whitham D. Reeve

Logic & Monitoring Components Evaluation

This document provides analyses of the logic components used in the existing Rev. G and H ARX and proposed for use in the Rev. I ARX. Refer to the Rev. I ARX block diagram for reference (see Reports folder).

Logic components: Because of the need for compatibility with the existing control system and associated software, the control logic for the Rev. I ARX is almost identical to that used in the Rev. G ARX. The Rev. H logic is considerably different but does include useful monitoring functions, which are adopted as described in the next section below.

The Rev. G ARX uses the 4-wire Serial Peripheral Interface (SPI) to control eight 20-port I/O expander integrated circuits (IC, MAX7301) through a buffer/driver IC (74LVC16244A). Each I/O expander controls the two polarizations A and B of an antenna stand, thus controlling 16 receiver channels on each ARX PCB. This basic configuration is adopted without change.

The Rev. G ARX used only 18 of the 20 ports on the I/O expander. These unused ports are used in the Rev. I ARX to add some control functionality, specifically 0.5 dB attenuator resolution (attenuator AT3 only) and an ARX board identification LED. The latter provides a flashing LED that may be used to identify the ARX board associated with a certain antenna stand or other function common to a single ARX PCB.

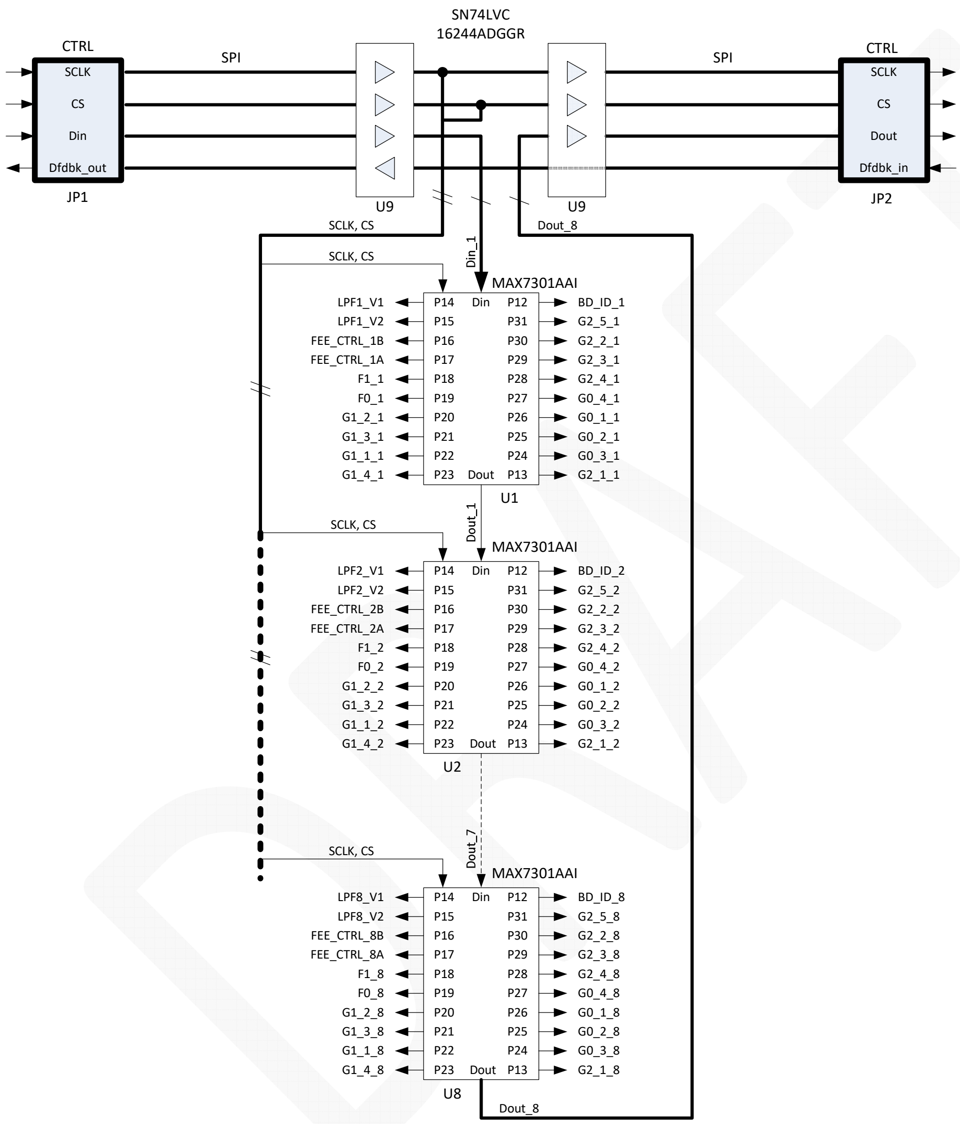
All switches and attenuators, except the HPF filter bank switches, are controlled by a dedicated port on the I/O expander. The HPF filter bank switches use four control pins, one for each position of the SP4T switch, so a 74LVC139 dual 2-4 line decoder is used to derive the four control lines from 2 control bits. Each decoder IC controls two channels.

The port assignments on the first I/O expander in the Rev. I ARX are shown in the table below (note that the ports/pins on the 20-port I/O expander are designated P12 – P31). The assignments are incremented for each additional I/O expander.

Pin	Assignment	Function
P12	BD_ID_1	Board Identification
P13	G2_1_1	Gain Cont. Atten. AT3 C0.5
P14	LPF1_V1	SPDT Pin 1
P15	LPF1_V2	SPDT Pin 2
P16	FEE_CTRL_1B	FEE Pwr Cont. 1B
P17	FEE_CTRL_1A	FEE Pwr Cont. 1A
P18	F1_1	SP4T Bin. Dec. Pin 1
P19	F0_1	SP4T Bin. Dec. Pin 2
P20	G1_2_1	Gain Cont. Atten. AT2 C4
P21	G1_3_1	Gain Cont. Atten. AT2 C8
P22	G1_1_1	Gain Cont. Atten. AT2 C2
P23	G1_4_1	Gain Cont. Atten. AT2 C16
P24	G0_3_1	Gain Cont. Atten. AT1 C8
P25	G0_2_1	Gain Cont. Atten. AT1 C4
P26	G0_1_1	Gain Cont. Atten. AT1 C2

P27	G0_4_1	Gain Cont. Atten. AT1 C16
P28	G2_4_1	Gain Cont. Atten. AT3 C4
P29	G2_3_1	Gain Cont. Atten. AT3 C2
P30	G2_2_1	Gain Cont. Atten. AT3 C1
P31	G2_5_1	Gain Cont. Atten. AT3 C8

The block diagram below shows the SPI and I/O expander hierarchy for the Rev. I ARX.



Truth tables:

TPS16412 : FEE power controller

Table 1. Truth Table : Positive logic: 0 = 0 V; 1 = +3 V

State	On	Off
Control	1	0

DAT-31A-PP+ : Attenuator

Truth Table : Positive logic: 0 = 0 V; 1 = +3 V

Attenuation	C16	C8	C4	C2	C1
Reference	0	0	0	0	0
1 (dB)	0	0	0	0	1
2 (dB)	0	0	0	1	0
4 (dB)	0	0	1	0	0
8 (dB)	0	1	0	0	0
16 (dB)	1	0	0	0	0
31 (dB)	1	1	1	1	1

Note: Not all 32 possible combinations of C1 - C16 are shown in table

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DAT-15R5A-PP+ : Attenuator:

Truth Table : Positive logic: 0 = 0 V; 1 = +3 V

Attenuation	C8	C4	C2	C1	C0.5
Reference	0	0	0	0	0
0.5 (dB)	0	0	0	0	1
1 (dB)	0	0	0	1	0
2 (dB)	0	0	1	0	0
4 (dB)	0	1	0	0	0
8 (dB)	1	0	0	0	0
15.5 (dB)	1	1	1	1	1

Note: Not all 32 possible combinations of C0.5 - C8 are shown in table

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HMC194A : SPDT RF switch for LPF:

Truth Table : Positive logic: 0 = 0 V; 1 = +3 V

Control		**RF Path**	
A	**B**	**RF – RF1**	**RF – RF2**
0	1	ON	OFF
1	0	OFF	ON
		70 MHz	**80 MHz**

PE42540 : SP4T RF switch for HPF:

Truth Table : Positive logic: 0 = 0 V; 1 = +3 V

Control		**RF Path**			
V1	**V2**	**RF – RF1**	**RF – RF2**	**RF – RF3**	**RF – RF4**
0	0	ON	OFF	OFF	OFF
1	0	OFF	ON	OFF	OFF
0	1	OFF	OFF	ON	OFF
1	1	OFF	OFF	OFF	ON
		3 MHz	**10 MHz**	**20 MHz**	**30 MHz**

Document Information

Author: Whitham D. Reeve

Revisions: 0.0 (Original draft started, 23 Apr 2023)
- 0.1 (Updated Rev. H control, 25 Apr 2023)
- 0.2 (Added truth tables, 29 Apr 2023)
- 0.3 (Updated monitoring for board temperature, 30 Apr 2023)
- 0.4 (Truth table check, 19 May 2023)
- 0.5 (Removed system block diagram, moved Monitoring section to a separate document, 29 Sep 2023)

Word count: 854

File size (bytes): 57875

Memo Cover Sheet

ARX-Eval-03

ARX Power Evaluation
29 September 2023
Whitham D. Reeve

ARX Power Evaluation

Whitham D. Reeve

This document provides analyses of the voltage regulating components used in the existing Rev. G and H ARX and those proposed for use in the Rev. I ARX. It includes thermal and heat dissipation calculations, a power system block diagram and description of the power supply input protection circuits proposed for the Rev. I ARX.

ARX Input and Bus Voltages:

The Rev. G ARX used 8 Vdc to power all on-board components through separate 3, 5 and 7 V voltage regulators and 15 Vdc to power the Front End Electronics. The 3 and 5 V circuits powered the logic and RF switching circuits and the 7 V circuit powered the GALI-74+ amplifiers. The Rev. H ARX used 5 Vdc for all on-board components including the ABA-54563-BLKG amplifiers and 15 Vdc for the FEE.

To avoid replacing expensive power supplies and maintain compatibility with the existing stations that use the Rev. G ARX, the 8 V and 15 V input voltage buses are unchanged in the Rev. I ARX. To improve the operating margin, the 8 V power supplies are adjusted to 8.8 V for both the Rev. G and Rev. I ARX (but still referred to as the 8 V bus). Additional changes recommended to improve the operating margin are described later.

The 5 V bus is not required in the Rev. I ARX PCB, and the 8 V input to the PCB is stepped down by a linear voltage regulator to 3.3 V for the logic, RF switching and monitoring circuits and to 7.0 V for the amplifiers. Although the amplifier voltage in the Rev. I ARX is the same as the Rev. G ARX, the voltage regulation in Rev. I in combination with the higher input voltage provides overall higher operating margin for the amplifiers.

Altitude Derating:

Thermal and power dissipation calculations are used to determine if a device is able to meet specific application conditions without overheating. In the case of the LWA installations in New Mexico and elsewhere, it is necessary to evaluate the heat dissipation at high altitudes because the thinner air at high altitudes reduces the ability of electronic devices to dissipate heat. The operating altitude of the LWAs in New Mexico is on the order of 7000 ft (2100 m) and the Rev. I ARX will be deployed at sites with altitudes as high as 10 000 ft (3000 m).

Altitude meter	Altitude feet	Derating factor
0	0	1.00
500	1640	0.97
100	3280	0.94
1500	4920	0.91
2000	6560	0.89
2500	8200	0.86
3000	9840	0.83
3500	11480	0.81
4000	13120	0.78

The derating factor for high altitudes is discussed in a Texas Instruments application note (see References) but altitudes only to 8350 ft are listed. However, the TI derating factors are comparable at most altitudes to those given in a design note from Flex Power Modules (FPM) for forced air cooling (see table). The FPM data extends to 13 120 ft.

Note that the FPM derating factors are the inverse of the derating factors used in the calculations. The TI factor for 2100 m (7000 ft) altitude is 1.17 and higher than the (interpolated)

FPM factor for the same altitude, so the TI factor is used for that altitude. The FPM factor is used for 3000 m (9840 ft) altitude and is (1/0.83 =) 1.20.

Thermal Control on a PCB: The thermal calculations described below are based on standard PCB dimensions and layer configurations and using the PCB itself as a heatsink. No external heatsinks are used on the power management devices. To ensure the actual ARX PCB is adequate as a heatsink, the following recommendations from a Texas Instrument Tech-Days presentation (*You Think LDOs are Simple?*, see References) are implemented:

- ✓ Use as much metal (copper) as possible in the areas around the device, on the same layer and the layers below it;
- ✓ The more thermal vias the better for spreading the heat between the different layers;
- ✓ Place the largest possible array of thermal vias in the thermal pad to maximize the amount of heat that can be transferred from the device to the internal and bottom layers;
- ✓ A 6x6 via array allows the internal layers to dissipate heat almost as well as the top layer which may be crowded with other components;
- ✓ Make vias as small as possible to decrease the amount of open space in the via hole;
- ✓ If the power pad is too small to place many vias, then placing extra vias as close as possible to the power pad is still helpful.

Logic and Control Power Bus:

Voltage: All logic and control devices are selected to operate at 3.3 V.

3.3 V Bus Load: The load on the 3.3 V bus consists of the following integrated circuits; all loads are estimated:

Type	Qty per PCB	Unit load (mA)		Total load per PCB (mA)
DAT-31A-PP+ digital step attenuator	16 x 2 = 32	0.230		7.36
DAT-15R5A-PP+ digital step attenuator	16 x 1 = 16	0.230		3.68
MAX7301AAI I/O expander	16 x 1/2 = 8	0.270		2.16
74LVC16244ADGGR buffer/driver	16 x 1/16 = 1	24		24.0
HMC194A LPF switch	16 x 2 = 32	0.05		1.60
PE42540 HPF switch	16 x 2 = 32	0.160		5.12
Diagnostics microprocessor	1	?		25 (guess)
Diagnostics support ICs	?	?		5 (guess)
AD8361 RF power detector	16	1.1		17.6
			Total	91.64

The 3.3 V bus design load of 92 mA is increased to 200 mA to account for the uncertainty in the diagnostic components and to provide some margin. The performance requirements in terms of line and load regulation and dropout voltage for the 3.3 V voltage regulator are not critical.

Voltage Regulator Device 3.3 V Bus: The Texas Instruments TLV1117 LDO regulator with fixed 3.3 V output (TLV1117-33xxx) was evaluated to power the 3.3 V bus but its thermal characteristics turned out to be unsuitable for the load conditions. The Rohm BDxxC0A-C series was then evaluated and the BD33C0AFP with fixed 3.3 V output and TO252-3 package was selected. The maximum recommended input voltage is 26.5 V, maximum output current is 1 A and maximum dropout voltage is 0.5 V. In the ARX application, the input voltage is 8.8 V and load current is estimated 200 mA maximum (see above).

3.3 V Bus Thermal Calculations: The estimated thermal performance is based on the junction-to-air (also referred to as junction-to-ambient) thermal resistance $R_{\theta JA}$. According to the datasheet, $R_{\theta JA}$ = 23 °C/W for the TO252-3 package. The maximum allowable junction temperature is 125 °C, and the quiescent current (called circuit current in the Rohm datasheet, see References) for the BD33C0AFP can be as high as 2.5 mA.

The power that can be dissipated P_d by the device must be ≥ the power consumed P_c by the device. The power consumed is

$$P_c = (V_{IN} - V_{OUT}) \cdot I_{OUT} + V_{IN} \cdot I_q$$

where V_{IN} and V_{OUT} are the input and output voltages (V), I_{OUT} is the load current (A) and I_q is the voltage regulator quiescent current (A). For the BD33C0AFP in this application, V_{IN} = 8.8 V, V_{OUT} = 3.3 V, I_q = 2.5 mA, and

$$P_c = (V_{IN} - V_{OUT}) \cdot I_{OUT} + (V_{IN} \cdot I_q) = (8.8 - 3.3) \cdot 0.2 + (8.8 \cdot 0.0025) = 1.12 \text{ W}$$

The maximum power dissipation at sea level is

$$P_d = \frac{T_J - T_a}{R_{\theta JA}}$$

where T_J is the junction temperature (125 °C) and T_a is the ambient temperature. Assuming an operational maximum ambient temperature of 85 °C, the maximum power dissipation at sea level is

$$P_d = \frac{T_J - T_a}{R_{\theta JA}} = \frac{125 - 85}{23} = 1.74 \text{ W}$$

The maximum power dissipation at sea level is reduced by the factors 1.17 and 1.20 for 2100 and 3000 m altitudes, respectively. With these factors, the maximum power dissipation P_d = 1.74/1.17 = 1.49 W at 2100 m altitude and P_d = 1.74/1.20 = 1.45 W at 3000 m altitude. Therefore, $P_d > P_c$ (1.12 W) and, under the stated conditions, the BD33C0AFP device meets the thermal requirements.

Equivalent Series Resistance for 3.3 V Regulator Input and Output Capacitors: The datasheet for the BC33C0AFP regulator recommends X5R or X7R dielectrics when ceramic capacitors are used on the output and that the ESR be controlled on both the input and output capacitors. These input and output capacitor values and series resistors for ESR are To Be Determined. See Operation Note 15 in the datasheet and Rohm application note *BAxxCC0 Series Circuit Using a Ceramic Output Capacitor* listed in the References.

Amplifier Power Bus:

Voltage: As discussed below, the voltage regulators for 7.0 V amplifier power bus in the Rev. G ARX had no margin. The Rev. I ARX uses the same amplifiers. Each receiver channel uses three amplifiers, and each amplifier presents a nominal load of 80 mA giving a total load of 240 mA in each receiver channel. The Rev. G ARX PCB used two LM1084 voltage regulators, and the load was split with 8 receiver channels on each regulator. Thus, the design load on each Rev. G voltage regulator was 8 x 0.24 A = 1.92 A.

Rev. G ARX PCB Power Dissipation: Neglecting the 3.3 V and 5.0 V loads and only considering the 7.0 V amplifier loads:

The total amplifier load current on each Rev. G PCB is 2 x 1.92 A = 3.84 A. The total power consumed by the amplifiers including bias resistors is 7.0 V x 3.84 A = 26.9 W.

Each voltage regulator has a quiescent current of 10 mA. Power losses in the two voltage regulators assuming 8.0 V input and 7.0 V output are (1.0 V x 3.84 A) + (1.0 V x 0.01 A x 2) = 3.86 W.

The total power input per PCB is 26.9 W + 3.9 W = 30.8 W, and the total input current is 30.8 W/8.0 V = 3.85 A/PCB.

8.0 V Input Bus Voltage Drop: Per Zoom meeting of 5 Sep 2023, the ARX power cables are 12 or 14 AWG (not sure which), lengths are approx. 5 ft and each cable serves 4 ARX PCBs. Therefore, the load per power wiring circuit cable is 4 PCBs x 3.85 A/PCB = 15.4 A. This value does not include current to the 3.3 and 5.0 V circuits on the Rev. G ARX PCB.

The power wiring is assumed to be tinned 19 strand/27 AWG, 14 AWG copper or tinned 19 strand/25 AWG, 12 AWG copper. Looking first at 14 AWG as worst-case:

The dc resistance at 20 °C for tinned, 19 strand/27 AWG, 14 AWG copper wire is 3.05 ohms/1000 ft. The loop length is 10 ft, giving a loop resistance of 0.0305 ohms. The voltage drop in the power wiring at 20 °C is 15.4 A x 0.0305 ohms = 0.47 V. Since the station runs hotter than 20 °C, the wire resistance will be somewhat higher, and the voltage drop also will be somewhat higher. Assuming the wire temperature is 40 °C (104 °F), the resistance will be 0.0329 and the voltage drop will be 15.4 A x 0.0329 ohms = 0.51 V. For reference, the calculation of copper wire resistance as a function of temperature is:

$$R_T = R_{ref} \cdot \left[1 + \alpha \cdot \left(T - T_{ref}\right)\right]$$

where R_T is the wire resistance at any temperature T, R_{Ref} is the resistance at the reference temperature T_{Ref}, and α is the temperature coefficient of resistance. For copper, α = 0.004 / °C at practical operating temperatures. T_{Ref} is given in copper wire properties tables (usually 20 °C) along with R_{Ref}.

Considering power wiring voltage drop at the assumed 40 °C operating temperatures, the input voltage to the Rev. G PCBs is not 8.0 V but closer to 7.5 V. The typical dropout voltage of the LM1084 is 1.0 V and can be as high as 1.5 V. Thus, with 8.0 V input voltage, the voltage regulators under worst-case conditions deliver around 6 V, which is considerably lower than the Rev. G design voltage of 7.0 V at the amplifier bias circuits. If the 3.3 V and 5.0 V loads are taken into account, the situation is worse because of the additional voltage drop in the power wiring circuit cables due to those load currents.

Increasing Power Wiring Size to 12 AWG: The dc resistance at 20 °C for tinned 19 strand/25 AWG, 12 AWG copper wire is 1.87 ohms/1000 ft and at 40 °C is 2.0196 ohms/1000 ft. The loop resistance for 10 ft loop length is 0.0187 and 0.020196 ohms, respectively. The voltage drop for a 15.4 A load is 15.4 A x 0.0187 ohms = 0.29 V at 20 °C and 15.4 A x 0.020196 = 0.31 V at 40 °C. Although the voltage drop is lower, the LM1084 voltage regulators are still starved in terms of input voltage as shown below.

ARX Rev. I Scenario 1 – Linear Technology LM1084 LDO Voltage Regulator: If the power supply output voltage is 8.0 V, then, as shown above, the voltage at the PCB with 14 AWG power wiring is 8.0 V – 0.51 V = 7.5 V and with 12 AWG power wiring is 8.0 V – 0.31 V = 7.7 V, both at 40 °C. The LM1084 regulator has a maximum 1.5 V dropout voltage under all conditions. For the worst-case with 14 AWG wiring, the LM1084 output will be 7.5 V – 1.5 V = 6.0 V, and with 12 AWG wiring will be 7.7 V – 1.5 V = 6.2 V. Both voltages are far below the required minimum recommended amplifier operating voltage of 7.0 V (see R BIAS table on pg 3 of Mini-Circuits GALI-74+ datasheet).

If the power supply voltage is increased to 8.8 V, the voltage at the PCB with 14 AWG power wiring will be 8.8 V – 0.51 V = 8.3 V and with 12 AWG power wiring is 8.8 V – 0.31 V = 8.5 V, both at 40 °C. For the worst-case with 14 AWG wiring, the LM1084 output will be 8.3 V – 1.5 V = 6.8 V and with 12 AWG wiring will be 8.5 V – 1.5 V = 7.0 V. Even with the elevated input voltage, the 14 AWG power wiring does not meet the design goal of 7.0 V at the amplifiers, whereas the 12 AWG wiring provides the needed voltage but has no margin.

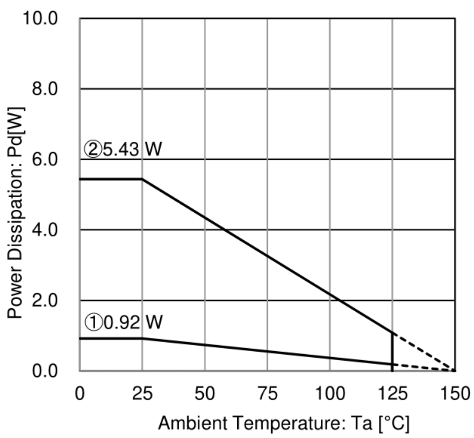
ARX Rev. I Scenario 2 – Rohm BDxxC0Axx LDO Voltage Regulator: The Rohm BDxxC0AFP LDO voltage regulator datasheet specifies a maximum dropout voltage of 0.5 V but recommends an operating input voltage of V_{Out} + 1 V (see Recommended Operating Conditions on pg 7/43 of datasheet). If the power supply voltage is increased to 8.8 V, the voltage at the PCB with 14 AWG power wiring will be 8.8 V – 0.51 V = 8.3 V and with 12 AWG power wiring will be 8.8 V – 0.31 V = 8.5 V, both at 40 °C.

If the LDO output voltage (and the amplifier operating voltage) is supposed to be 8.0 V, the input must be at least 9.0 V, which is not achievable with nominal 8 V power supplies having ±10% adjustment range. However, by reducing the LDO output voltage (and amplifier operating voltage) to 7.0 V, the LDO requires 8.0 V input voltage. This is achievable and provides at least some margin under relatively high temperature conditions (40 °C) with 14 AWG power wiring. Using 12 AWG power wiring, the margin is increased by 0.2 V.

This scenario has been selected and further supported by the following thermal calculations. As mentioned above, the lowest recommended operating voltage for the amplifiers is 7.0 V, which requires an adjustable LDO voltage regulator because 7.0 V is not a standard fixed regulator output voltage. Therefore, for this application, the adjustable BD00C0AWFP in the TO252-5 package will be used.

Thermal Calculations for Rohm BDxxC0A Regulator: As discussed above, the operating altitude of the LWAs in New Mexico is on the order of 7000 ft (2100 m) and future LWAs will be deployed near 10 000 ft (3000 m). At higher altitudes, it is necessary to derate the voltage regulator junction-to-ambient thermal resistance θ_{JA} values determined at sea level (derating makes θ_{JA} values larger and is equivalent to reducing the allowable power dissipation). The discussion below first calculates sea level conditions and then applies the derating for operation at 7000 ft and 10 000 ft altitudes.

The thermal calculations assume a 4-layer FR4 PCB with two signal and two power (2s2p) layers, TO252-5 package (condition 2 in the plots from the datasheet figure 74 below) and sea level. For these conditions, junction-to-ambient thermal resistance θ_{JA} = 23 °C/W. The maximum device current is 1 A and its maximum dropout voltage is given as 0.5 V but, as mentioned above, Rohm recommends that the device input voltage exceeds the desired output voltage by at least 1 V.



Each Rohm LDO voltage regulator will supply two receiver channels. Each channel contains three amplifiers, giving a total of six amplifiers per voltage regulator. Therefore, the operating current of each LDO will be 6 amplifiers x 0.08 A/amplifier = 0.48 A, rounded to 0.5 A to provide some margin.

The allowable power dissipated P_d must be ≥ the power consumed P_c by the voltage regulator The power consumed is

$$P_c = (V_{IN} - V_{OUT}) \cdot I_{OUT} + V_{IN} \cdot I_q \text{ W}$$

where V_{IN} and V_{OUT} are the input and output voltages (V), I_{OUT} is the load current (A) and I_q is the voltage regulator quiescent (or circuit) current (A). Assuming the BD00C0AWFP is used in this application:

14 AWG power wiring at 40 °C: V_{IN} = 8.3 V, V_{OUT} = 7.0 V, input-output differential = 1.3 V, I_{OUT} =0.5 A, and I_q = 2.5 mA:

$$P_c = (V_{IN} - V_{OUT}) \cdot I_{OUT} + (V_{IN} \cdot I_q) = (8.3 - 7.0) \cdot 0.5 + (8.3 \cdot 0.0025) = 0.671 \text{ W}$$

12 AWG power wiring at 40 °C: V_{IN} = 8.5 V, V_{OUT} = 7.0 V, input-output differential = 1.5 V, I_{OUT} =0.5 A and I_q = 2.5 mA:

$$P_c = (V_{IN} - V_{OUT}) \cdot I_{OUT} + (V_{IN} \cdot I_q) = (8.5 - 7.0) \cdot 0.5 + (8.5 \cdot 0.0025) = 0.771 \text{ W}$$

The maximum power dissipation P_d at sea level is

$$P_d = \left[\frac{(T_J - T_a)}{R_{\theta JA}} \right] \text{W}$$

where T_J is the junction temperature and T_a is the ambient temperature. Assuming a maximum ambient temperature of 85 °C, the maximum power dissipation at sea level is

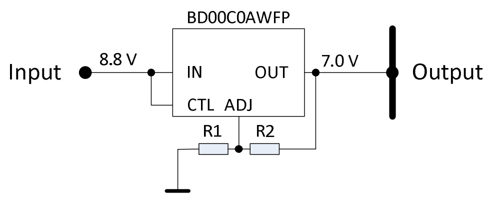
$$P_d = \left[\frac{(125°C - 85°C)}{23} \right] = 1.74 \text{ W}$$

The maximum power dissipation at sea level is reduced by the factors 1.17 and 1.20 for 2100 and 3000 m altitudes, respectively. With these factors, the maximum power dissipation is P_d = 1.74 W/1.17 = 1.49 W at 2100 m altitude and P_d = 1.74 W/1.20 = 1.45 W at 3000 m altitude. Therefore, P_d > P_c (0.671W for 14 AWG wiring and

0.771 W for 12 AWG wiring) and, under the stated conditions, the BD00C0AWFP device meets the thermal requirements.

Equivalent Series Resistance for 7.0 V Regulator Input and Output Capacitors: The datasheet for the BC00C0AWFP regulator recommends X5R or X7R dielectrics when ceramic capacitors are used on the output and that the equivalent series resistance (ESR) be controlled on both the input and output capacitors. These input and output capacitor values and series resistors for ESR are To Be Determined. See *Operation Note 15* in the datasheet and Rohm application note *BAxxCC0 Series Circuit Using a Ceramic Output Capacitor* listed in the References.

Resistive Voltage Divider for Rohm Variable Voltage Regulators: To set the output voltage, the ADJ pin of the BC00C0AWFP voltage regulators is connected to the resistive voltage divider shown below. The designations R1 and R2 are the same as used in the device datasheet.



Output voltage Vout ≈ ADJ × (R1+R2) / R1, where ADJ is the Adjust Terminal Voltage (reference voltage) and R1 and R2 are the voltage divider resistances. According to the datasheet, the ADJ pin, or reference voltage, is typically 0.75 V but can vary from 0.742 to 0.758 V. To limit offset voltage due to the ADJ pin current, the recommended range for R1 is 5k to 10k. Rearranging the output voltage equation for R2 gives R2 = [(Vout x R1) / ADJ] – R1.

For 7.0 V output, the Rohm application note (*Table of resistance for output voltage setting on linear regulator ICs*, see References), Table 1, shows R1 = 8.2k and R2 = 68k. These values assume ADJ = 0.75 V and do not account for possible variations in the ADJ pin voltage. The goal of this design is to not let the amplifier bias voltage go below 7.0 V. If the ADJ pin voltage is worst-case (ADJ = 0.742 V), then R2 = 69.1k. The nearest standard 1% value in size 0805 is 69.8k. However, this does not account for the R1 and R2 resistor tolerances (±1%) and ADJ pin voltage variation.

For worst-case calculations, the nominal value of R1 is assumed to be 8200 ohms (for example, Bourns p/n CR0805-FX-8201ELF). R1 can vary ±82 ohms from 8118 to 8282 ohms due to its tolerance. The worst-case in terms of maintaining at least 7.0 V output voltage is a high value for R1 and a low value for ADJ. For this situation, R2 must be ≥ 69.85k, which is not a standard value. The nearest standard 1% value higher than 69.85k is 71.5k (for example, Bourns p/n CR0805-FX-7152ELF). R2 can vary ±715 ohms from 70 785 to 72 215 ohms due to its tolerance.

The lowest regulator output voltage occurs when R1 is highest, R2 is lowest and ADJ is lowest; in this case, Vout = 7.08 V, which meets the design goal stated above. The highest regulator output voltage occurs when R1 is lowest, R2 is highest and ADJ is highest; in this case, Vout = 7.5 V. When all values are nominal, the regulator output voltage is 7.35 V. All voltages are acceptable for biasing the GALI-74+ amplifiers when it is set for a bias voltage of 7.0 V.

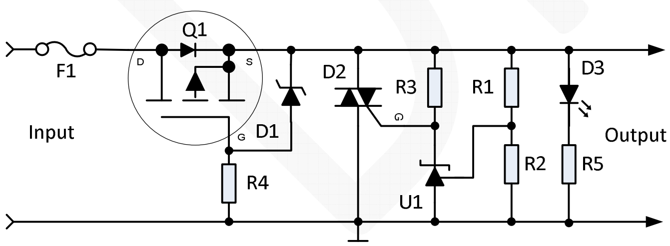
Note: Changes in the voltage divider resistances due to temperature variations are assumed to be smaller than variations due to tolerances. Also, an LDO output voltage = 7.35 V is higher than the nominal output of 7.0 V and implies lower available input margin (the input would have to be 0.35 V higher for 7.35 V output than for 7.0 V output under worst-case conditions). Although the Rohm datasheet specifies a maximum dropout of 0.5 V, it recommends that the input exceed the output by 1 V, and the 1 V value was used in all the previous voltage drop calculations. Thus, the needed margin is intact with the datasheet maximum dropout voltage.

<u>Voltage Regulator Locations on PCB</u>: It is desirable to locate the 7.0 V voltage regulators so that their power is dissipated uniformly across the PCB. The power dissipation of the eight voltage regulators will be nearly equal, differing mainly due to component tolerances. The goal is to reduce the differences in channel gain due to temperature differentials between receiver channels. This might be achieved by locating each voltage regulator at the top of the PCB directly in line with the two receiver channels it serves.

<u>Increasing the Operating Margin</u>: Upgrading the power wiring from 14 AWG to 12 AWG is recommended to improve the voltage regulator margins. Another improvement is to install remote voltage sensing (also called 4-wire sensing) on the 8 V power supply. The power supply is Artysen model IVS1-5I0-2I0-60-A and, when used with remote voltage sensing, it is able to compensate up to 0.5 V voltage drop in the wiring between the power supply output terminals and load terminals. The load voltage would be sensed, and regulated, at the end of the daisy-chained 8 V power wiring where the sense leads would be connected. Although not analyzed as part of the ARX power evaluation, the 15 V bus also may benefit from remote voltage sensing. This power supply is the Artysen model IVS1-5N0-3N0-60-A.

Input Voltage Protection:

The 8 V and 15 V inputs on the ARX PCB are each equipped with the reverse polarity and overvoltage crowbar circuit shown below. The body diode in MOSFET Q1, Zener diode D1 and R4 provide the reverse polarity guard function. During normal operation, the body diode of the MOSFET is forward-biased and conducts for a very short time until the MOSFET turns on when the gate voltage is pulled below the source voltage. D1 limits the gate-source voltage to a safe value to prevent damage to the MOSFET and R4 limits the current in D1. If the input polarity is reversed, the gate-source voltage is positive with respect to the input and the MOSFET turns off, protecting the downstream circuits from a negative voltage. The MOSFET has very low drain-source resistance when turned on, which provides very low voltage drop across it during normal operation.



R1 and R2 form a voltage divider to set the voltage of the programmable reference U1 to the desired crowbar trip voltage. The intrinsic reference voltage of U1 is 2.5 V. The trip voltage setting for the 8.8 V input is 12 V and for the 15 V input is 20 V. Below the crowbar trip voltage only a very small leakage current flows through R3, producing negligible voltage drop. The gate of Triac D2 is at the bus voltage and remains off. When the input voltage rises to the point where the voltage across R1 increases to 2.5 V (U1 reference voltage), U1 conducts and draws current through R3, which results in a voltage drop and reduced voltage at the gate of D2. When the voltage drop reaches nominal 1 V, Triac D2 turns on and latches and shorts the positive bus to ground. The resulting short circuit current flows through fuse F1, MOSFET Q1 and Triac D2 to ground and opens the fuse.

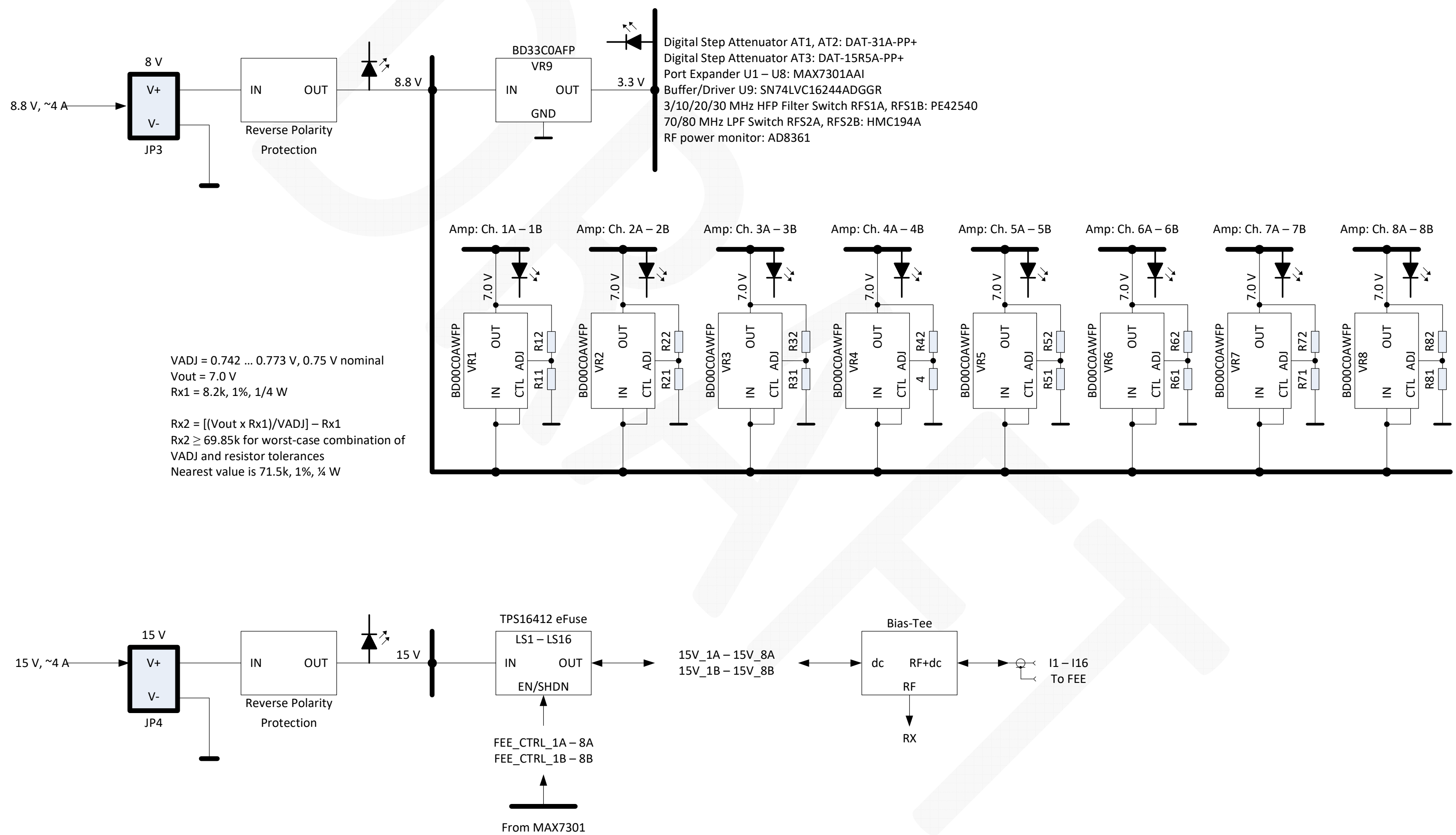
The programmable reference U1 output voltage (at U1 cathode) is

$$V_{Out} = V_{Ref} \cdot \left(1 + \frac{R1}{R2}\right) - I_{Ref} \cdot R1$$

where V_{Out} is the programmable reference output voltage, V_{Ref} is the device reference voltage (2.5 V) and I_{Ref} is the device leakage current (I_{Ref} < 4 µA). For most applications, I_{Ref} is assumed to be zero. R3 is set so that the current into D2 is limited to no more than 5 to 10 mA. The sum of R1 + R2 is in the range of 10 to 15 kOhm or to provide a current on the order of 1 mA. The fuse F1 current rating is 125 to 150% of the nominal load current to prevent nuisance opening. As previously discussed, the nominal load current on the 3.3 V bus is 0.2 A and on the 8 V bus is 8 voltage regulators x 0.5 A/voltage regulator = 4 A. Component values are shown in the table below (blank fields are To Be Determined for each voltage bus, 8 and 15 V).

Designation	**Device**	**8 V Bus**	**15 V Bus**	**Remarks**
F1	Fuse			ATM-series, automotive blade fuse
Q1	P-Channel MOSFET	BSC030P03NS3GAUMA1	BSC030P03NS3GAUMA1	30 V, 100 A, 3 mOhm
D1	Zener diode			
D2	Triac	T3035H-6G	T3035H-6G	D-PAK, 30 A, 35 mA max
D3	LED			Low current
U1	Programmable Ref.	TL431DBZ	TL431DBZ	SOT-23
R1	Resistor			
R2	Resistor			
R3	Resistor			
R4	Resistor			
R5	Resistor			

Power System Block Diagram:



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Document Information

Author: Whitham D. Reeve

Revisions: 0.0 (Original draft started, 24 Apr 2023)

0.1 (Added calculations for alt. 4 using Rohm and TI VR, 30 Apr 2023)

0.2 (Revised calcs for TO-252-3 voltage regulator, 02 May 2023)

0.3 (Completed 1st draft, 03 May 2023)

0.4 (Revised 8.0 V bus thermal analysis for 85 °C and 2100 m altitude, 29 Aug 2023)

0.5 (Added power block diagram, 3000 m altitude and packaging, 30 Aug 2023)

0.6 (Added 3.3 V bus thermal analysis, 03 Sep 2023)

0.7 (Added PCB heat dissipation, 04 Sep 2023)

0.8 (Replaced most of the section on amplifier bus voltage, 15 Sep 2023)

0.9 (Edits and added variable LDO voltage divider resistors, 16 Sep 2023)

1.0 (Distribution as Draft, 17 Sep 2023)

1.1 (12 AWG wiring upgrade, remote voltage sensing and LDO location, 19 Sep 2023)

1.2 (Distribution, 29Sep2023)

Word count: 4648

File size (bytes): 200372

Memo Cover Sheet

ARX-Eval-04

ARX Rev. I Filter Selection & Evaluation

29 September 2023

Whitham D. Reeve

ARX Rev. I Filter Selection & Evaluation
Whitham D. Reeve

1. Description:

This document describes the filter designs for the Rev. I ARX including methods, synthesis, simulation, and prototype construction and measurements. An appendix describes the filters used in the earlier ARX Rev. G and H.

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2. ARX Rev. I block diagram:

Refer to the master system block diagram in the Reports folder.

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3. Design methods:

Software:
The AADE Filter Design software synthesis and simulation tool was used to synthesize all filters according to the requirements described herein. The synthesis of each filter produced exact component values. The exact values were then replaced with the nearest catalog values, and AADE was used to simulate the filter characteristics and produce the plots shown in this document. Multiple prototypes of every filter were built.

Filter designs:
1) The Rev. I filters were simulated using Butterworth, Chebyshev and Elliptic types but only Butterworth and Elliptic were used in the initial and final designs;
2) Both Pi- and T-configurations were investigated for the highpass filters;
3) The tolerance for all inductor and capacitor values is ±2% and the inductor Q tolerance is ±20%;
4) The desirable self-resonant frequency (SRF) of the inductors is at least 10X the highest operating frequency (≥ 1 GHz SRF). However, this was not achievable in the high-value inductors required in the 3 MHz highpass filter, so inductors with SRF = 90 MHz (the highest available) were used in this filter. An alternative investigated during the prototype stage was to use smaller value, higher SRF inductors connected in series; however, the added SMD pad capacitance tended to reduce the filter return loss at the higher frequencies, so this idea was abandoned;
5) Coilcraft inductors in 0805 size were used in the designs where possible. Some 1008 size inductors were necessary to obtain the needed SRF or inductance value;
6) MLCC C0G (NP0) capacitors in size 0805 were used in all designs. C0G capacitors are relatively immune to capacitance variations due to voltage and temperature effects on the dielectric;
7) All filters are isolated from dc, which provides relief from capacitance changes caused by bias voltage on the dielectric. Similarly, inductance changes due to direct current are avoided;
8) Parallel capacitors and series inductors were not used in the initial designs to fine-tune the filter component values but were used in later designs for the prototypes; see also 4) above. Some final designs used parallel capacitors to obtain the needed capacitance;

9) The filter simulations addressed only insertion loss and return loss; phase and group delays were not analyzed;
10) Monte Carlo statistical analyses, in which component values are randomly varied within predetermined tolerances, are for most filters. The following tolerances are used with the Monte Carol method:
    - ✓ Input and output resistances: 10% (always real, never imaginary)
    - ✓ Inductors, Inductor Qs, and capacitors as noted is 3) above
11) The existing 83.7 MHz lowpass filter from the Rev. H ARX was retained for the Rev. I without any changes. All other filters were designed to meet the desired characteristics.

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4. Lowpass Filters:

The Rev. I ARX uses two lowpass filters with nominal cutoff frequencies of 73.5 and 83.7 MHz. The 73.5 MHz filter primarily is used to reject the FM broadcast band (88 to 108 MHz) whereas the 83.7 MHz filter provides a higher cutoff frequency at the expense of lower FM band rejection. The 73.5 MHz LPF may be referred to as a 70 MHz filter in the following discussions.

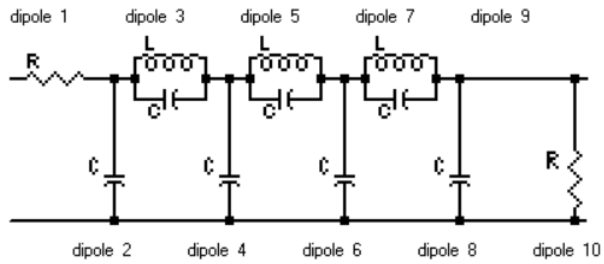
Several versions of the 73.5 MHz LPF were investigated including 5th order and 7th order Elliptic filters with frequencies between about 70 and 74 MHz. It was difficult finding a suitable combination of cutoff and stopband frequencies and passband return loss and stopband insertion loss that resulted in readily available inductor catalog values. The final design uses a 7th order Elliptic with a cutoff frequency of 73.5 MHz.

Although both lowpass filter designs use the Elliptic filter type, other filter types were evaluated including the Butterworth and Chebyshev; however, these generally did not provide the necessary roll off without using excessively high order. The Elliptic filter trades off ripple in both the passband and stopband for a steeper roll off in the stopband. The designed passband ripple was 0.1 dB for both lowpass filters. The lowpass Elliptic filter theoretically rolls off at approximately 10db/octave/order.

<u>73.5 MHz lowpass filter</u>:
The 73.5 MHz lowpass filter design criteria are:
Fc = 73.5 MHz with ≤ 0.1 dB ripple in the passband and at the cutoff frequency Fc
Fs = 91.5 MHz for design
Fs = 88 MHz achieved with ≥ 40 dB rejection

The 73.5 MHz lowpass filter is shown below with the nearest catalog component values.

Characteristics of the 73.5 MHz LPF from the simulation:
- ✓ Type: Elliptic
- ✓ Order: 7
- ✓ Attenuation at 70 MHz: 1.3 dB
- ✓ Attenuation at 88 MHz: 40.9 dB
- ✓ Attenuation at 108 MHz: > 40.9 dB
- ✓ Minimum return loss in passband: 16.6 dB at 52.2 MHz
- ✓ Return loss at 70 MHz: 18.3 dB



DIPOLE 1
R 1=50.

DIPOLE 2
C 2=47.pF

DIPOLE 3
C 3=6.pF
L 3=.14uHy
Qu~50.
F(L3C3)=
173.652279MHz

DIPOLE 4
C 4=68.pF

DIPOLE 5
C 5=30.pF
L 5=.1uHy
Qu~50.
F(L5C5)=
91.888149MHz

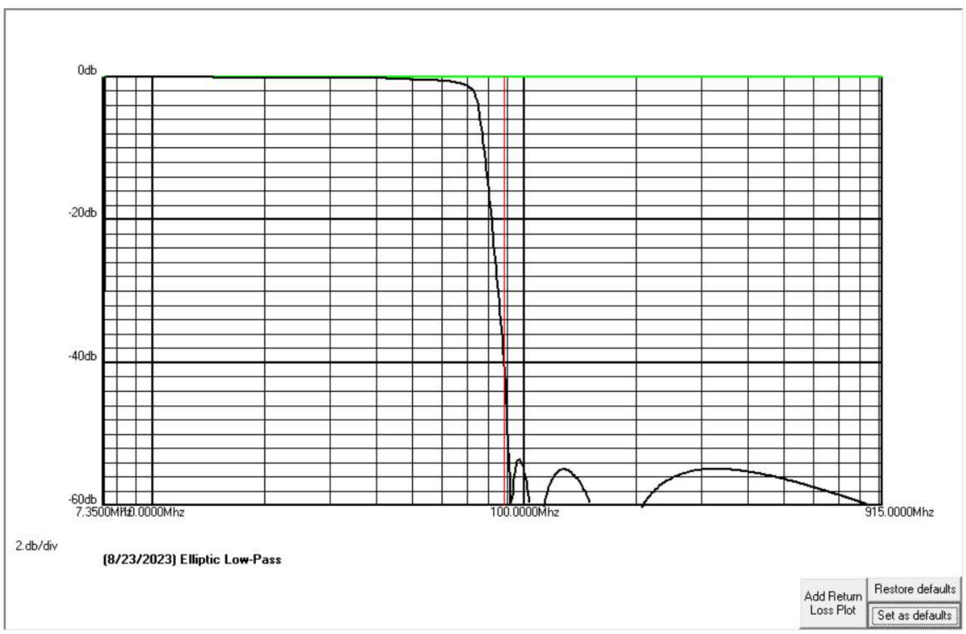
DIPOLE 6
C 6=58.pF

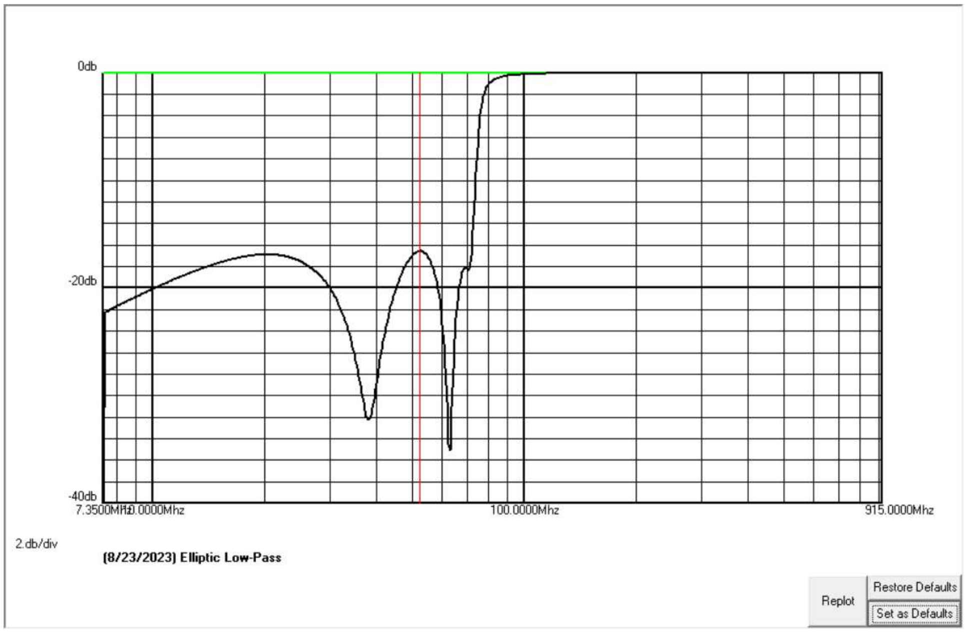
DIPOLE 7
C 7=22.pF
L 7=.1uHy
Qu~50.
F(L7C7)=
107.302241MHz

DIPOLE 8
C 8=33.pF

DIPOLE 10
R 10=50.

7.th order (8/23/2023) Elliptic Low-Pass
Cutoff = 100.m db @ 73.5Mhz
Stopband = 55.002 db minimum @ 91.5Mhz
Design Impedance=50. ohms
Input Impedance = 50. ohms
Output Impedance = 50. ohms
Capacitance Spread = C 4 : C 3 = 11.333
Inductance Spread = L 3 : L 5 = 1.4





<u>83.7 MHz lowpass filter</u>:

The 83.7 MHz lowpass filter design is a replication of the Rev. H 83.7 MHz lowpass filter:

Fc = 83.7 MHz with ≤ 0.1 dB ripple in the passband and at the cutoff frequency Fc (according to schematic)

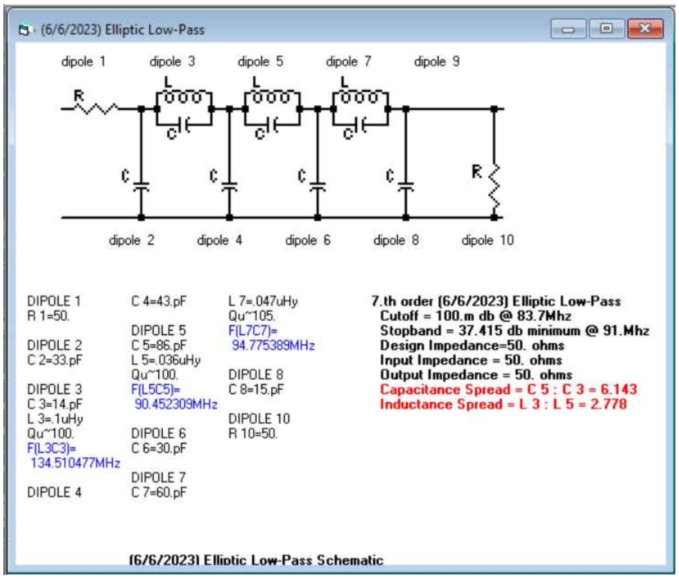
Fs =The stopband frequency Fs used in the original design is unknown

The filter is shown below with the component values from the original Rev. H schematics.

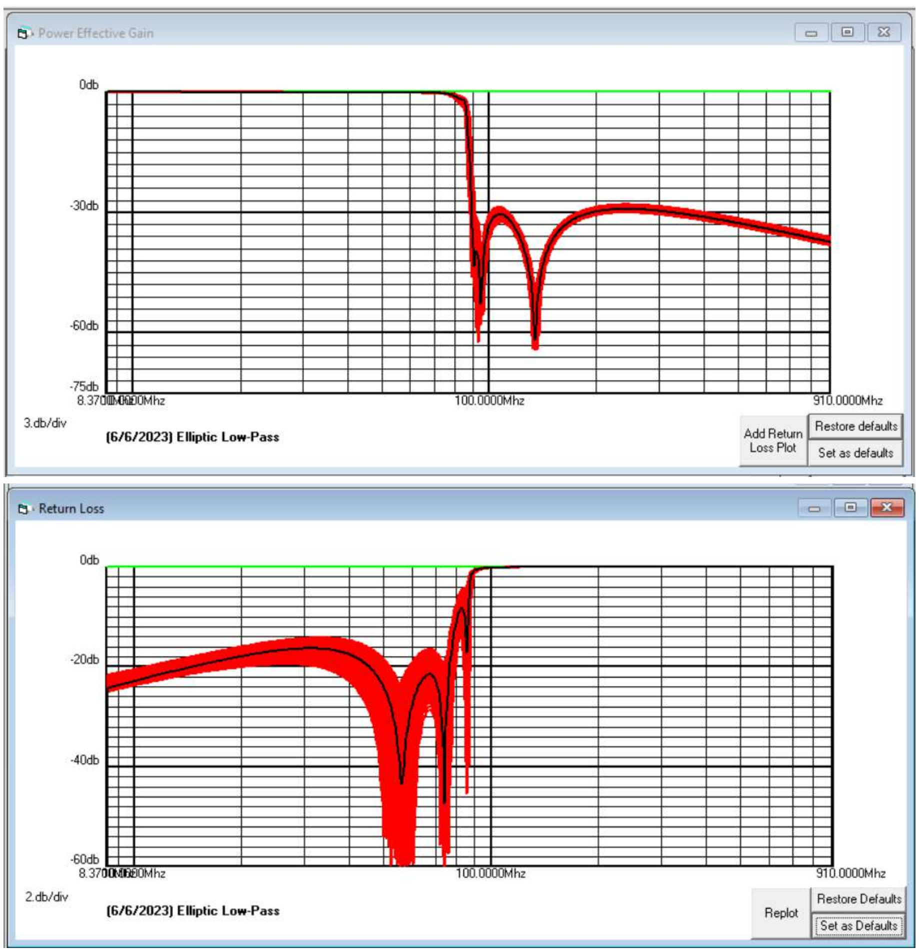
Characteristics of the final 83.7 MHz LPF from the simulations:

- ✓ Type: Elliptic
- ✓ Order: 7
- ✓ Attenuation at 88 MHz: 17.5 dB
- ✓ Attenuation at 108 MHz: 30.5 dB
- ✓ Minimum attenuation between 88 and 108 MHz: 17.5 dB at 88 MHz
- ✓ Minimum return loss in passband: 8.4 dB at 82.8 MHz
- ✓ Return loss at 88 MHz: 2.7 dB

Rev. H 83.7 MHz LPF Schematic:



Rev. H 83.7 MHz LPF Insertion Loss and Return Loss:



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5. Highpass Filters:

Four highpass filters with nominal cutoff frequencies of 3, 10, 20 and 30 MHz are used. The 3 and 10 MHz highpass filters generally are used for ionospheric research; one or the other is selected based on ionospheric conditions and observation requirements. The 3 MHz highpass filter provides moderate rejection of the medium frequency (MF) AM broadcast band. The 20 and 30 MHz filters allow celestial observations and are designed to reduce interference from HF radio traffic. The 20 MHz filter is a compromise that allows celestial observations when ionospheric conditions are relatively quiet, whereas the 30 MHz filter is specifically designed to reduce terrestrial interference from the Citizen Band Radio Service (CBRS) regulated under FCC Part 95. The CBRS frequency range is 26.96 to 27.41 MHz (including sidebands).

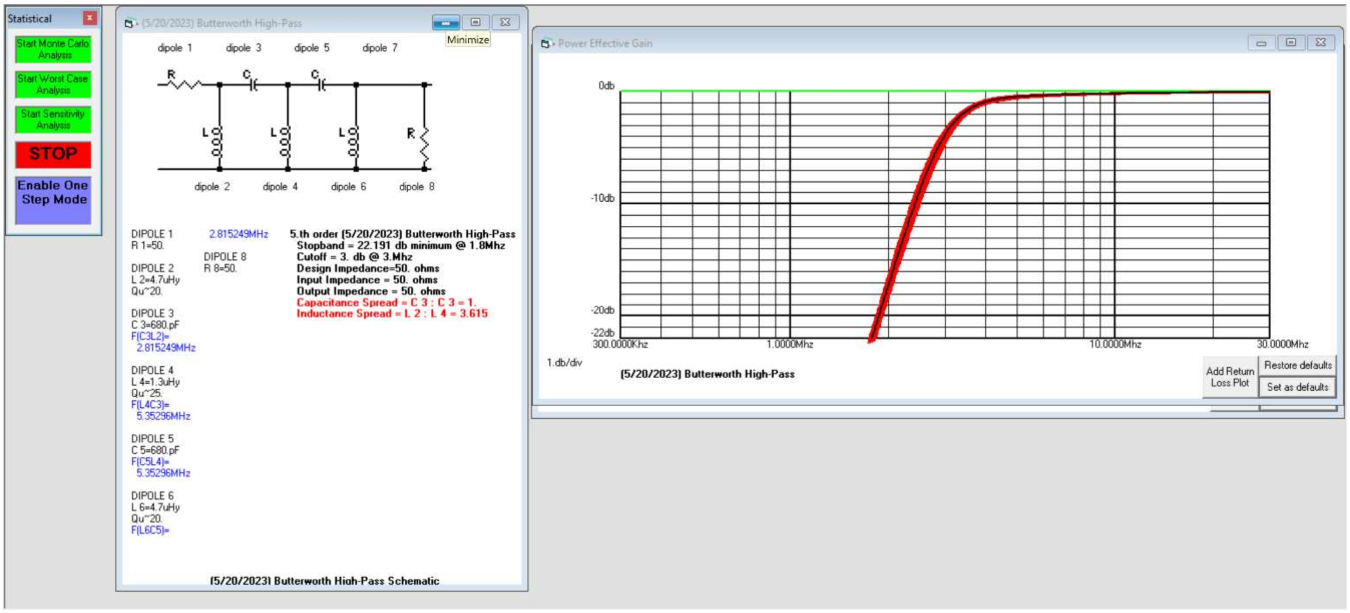
The proposed highpass filter designs are based on the Butterworth type for the 3, 10 and 20 MHz filters and Elliptic type for the 30 MHz highpass filter. The Butterworth filters exhibit a flat response in the passband and roll off at 6db/octave/order. The Elliptic filter trades off ripple in both the passband and stopband for a steeper roll off in the stopband, a characteristic necessary for rejecting the CBRS interference while still providing useful observation bandwidth. As with the lowpass Elliptic filters described previously, the highpass Elliptic filter theoretically rolls off at approximately 10db/octave/order.

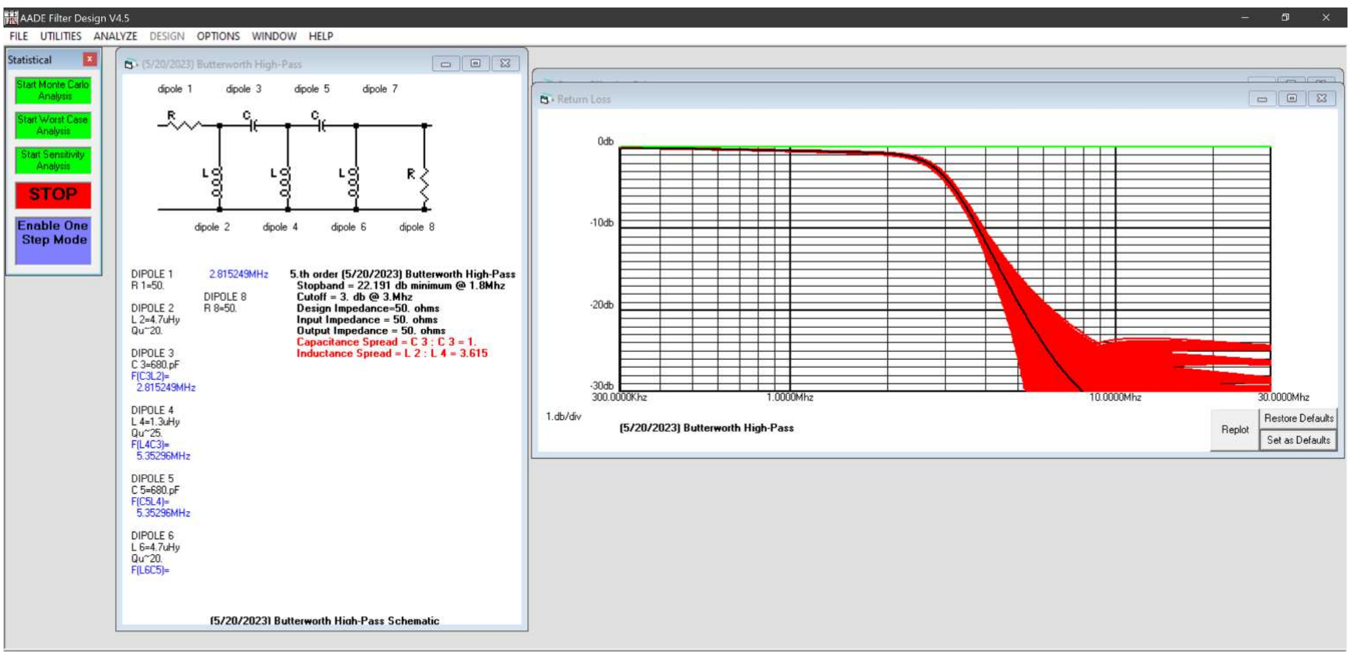
<u>3 MHz highpass filter</u>:
The 3 MHz highpass filter design criteria are:
Fc = 3 MHz with ≤ 3.0 dB attenuation at the cutoff frequency Fc
Fs = 1.8 MHz with ≥ 20 dB rejection in the stopband and at the stopband frequency Fs

The proposed 3 MHz filter is shown below with catalog component values. Also shown are the filter attenuation and return loss after Monte Carol statistical analysis.

Characteristics of the final 3 MHz HPF from the simulation with single catalog component values:

- ✓ Type: Butterworth
- ✓ Order: 5
- ✓ Attenuation at 3 MHz: 3.8 dB
- ✓ Attenuation at 1.8 MHz: 21.5 dB
- ✓ Return loss at 3 MHz: 3.8 dB
- ✓ Return loss at 4.5 MHz: 15.5 dB





<u>10 MHz highpass filter</u>:

The 10 MHz highpass filter design criteria are:

Fc = 10 MHz with ≤ 3.0 dB attenuation at the cutoff frequency Fc

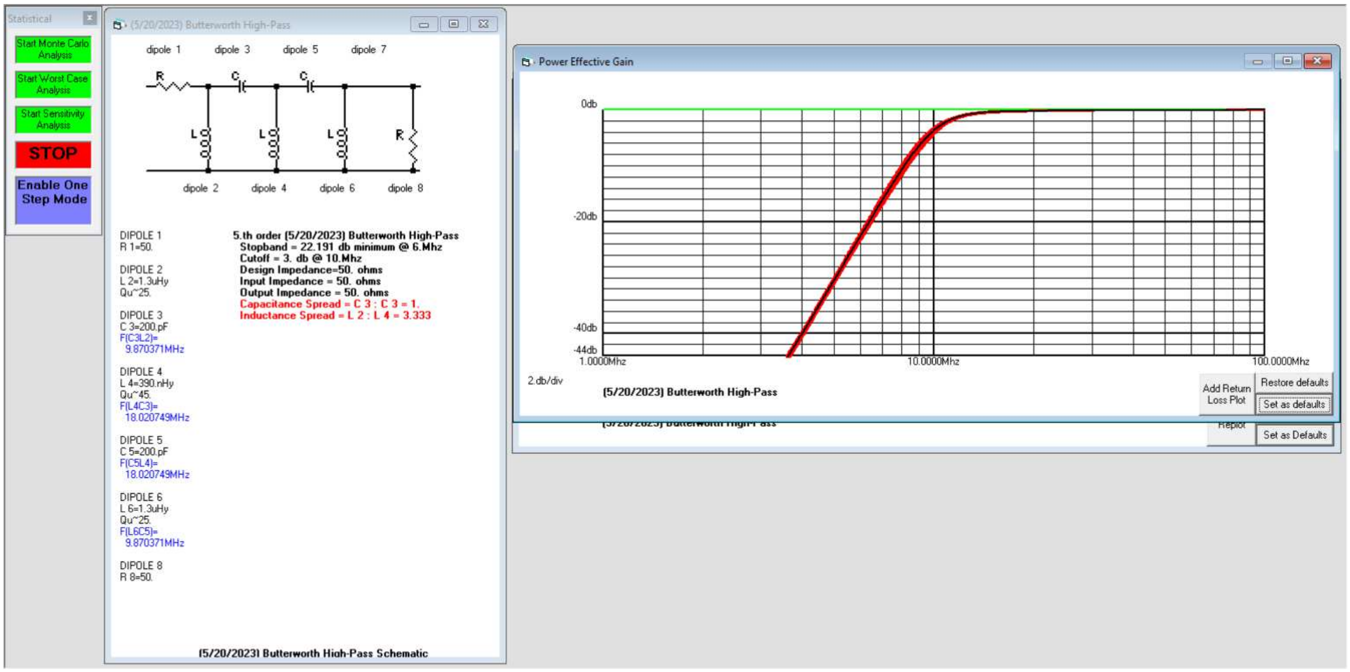
Fs = 6 MHz with ≥ 20 dB rejection in the stopband and at the stopband frequency Fs

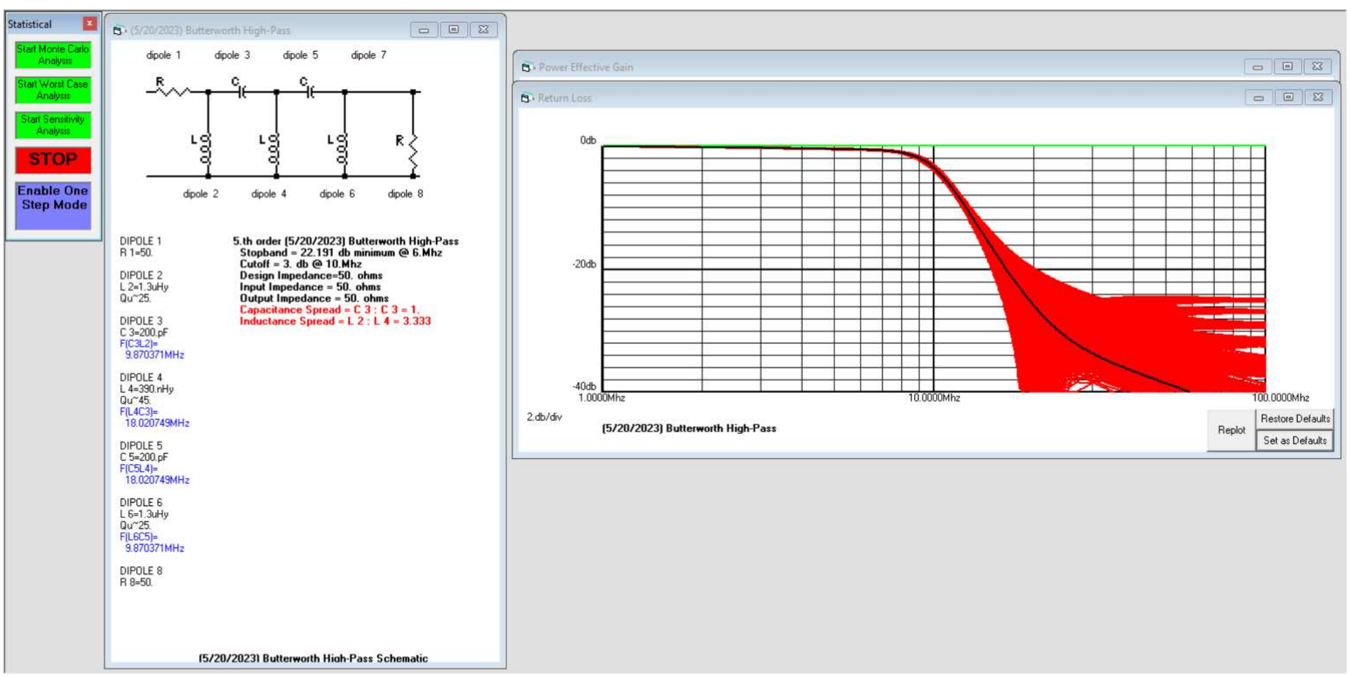
The proposed 10 MHz filter is shown below with catalog component values. Also shown are the filter attenuation and return loss after Monte Carol statistical analysis.

Characteristics of the final 10 MHz HPF from the simulation with single catalog component values:

- ✓ Type: Butterworth
- ✓ Order: 5

- ✓ Attenuation at 10 MHz: 3.6 dB
- ✓ Attenuation at 6 MHz: 22.5 dB
- ✓ Return loss at 10 MHz: 3.5 dB
- ✓ Return loss at 15 MHz: 16.6 dB





<u>20 MHz highpass filter</u>:

The 20 MHz highpass filter design criteria are:

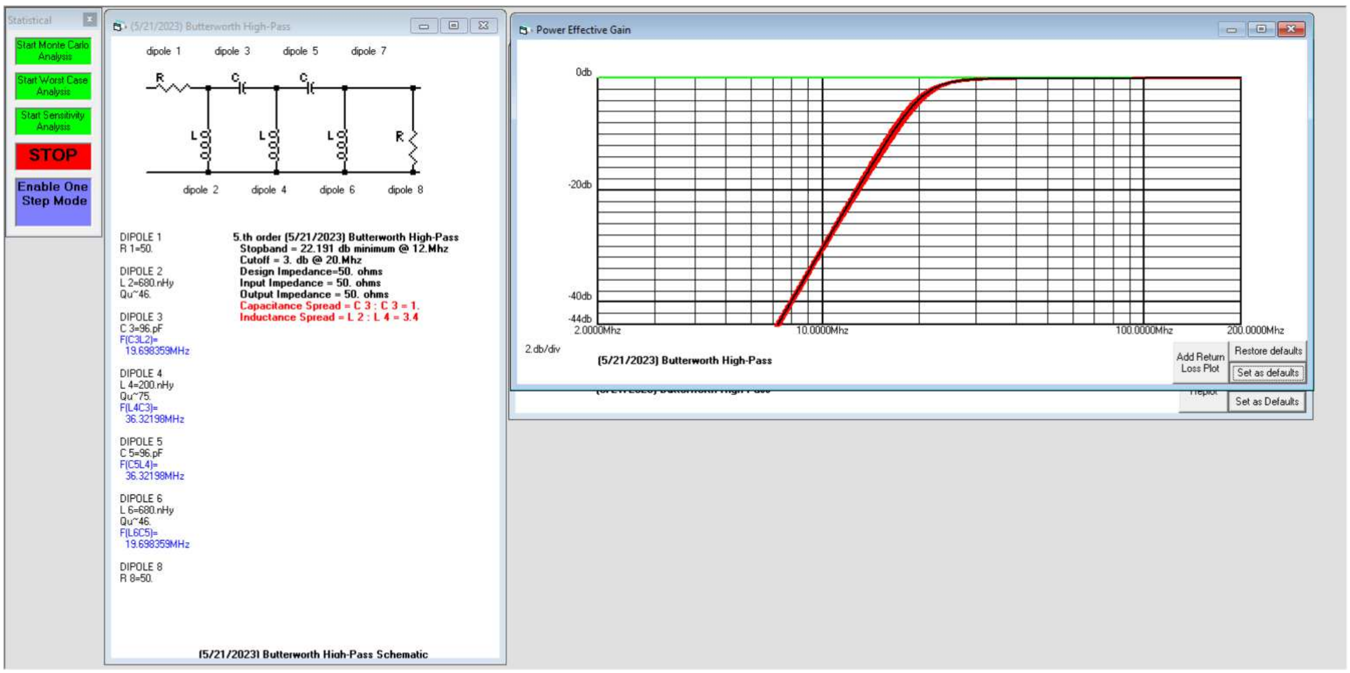
Fc = 20 MHz with ≤ 3.0 dB attenuation at the cutoff frequency Fc

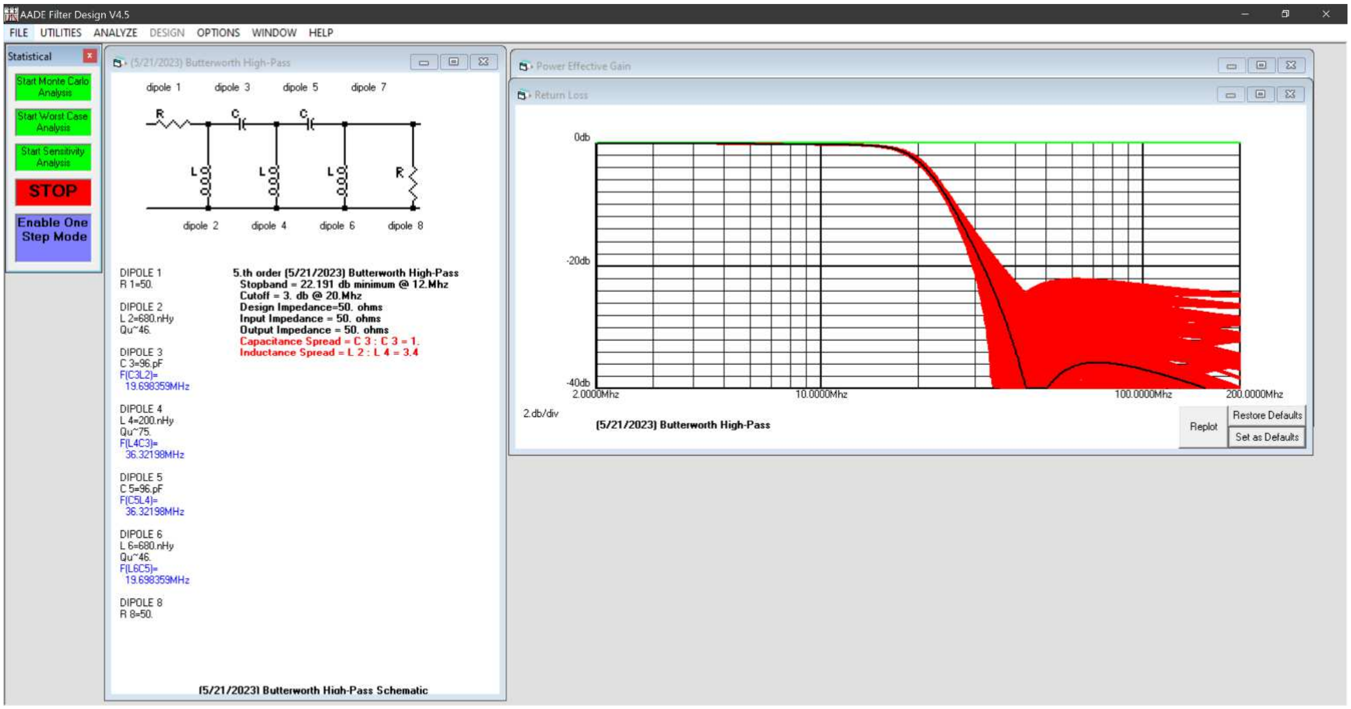
Fs = 12 MHz with ≥ 20 dB rejection in the stopband and at the stopband frequency Fs

The proposed 20 MHz filter is shown below with catalog component values. Also shown are the filter attenuation and return loss after Monte Carol statistical analysis.

Characteristics of the final 20 MHz HPF from the simulation with single catalog component values:

- ✓ Type: Butterworth
- ✓ Order: 5
- ✓ Attenuation at 20 MHz: 3.8 dB
- ✓ Attenuation at 12 MHz: 22.6 dB
- ✓ Return loss at 20 MHz: 2.9 dB
- ✓ Return loss at 30 MHz: 17.3 dB





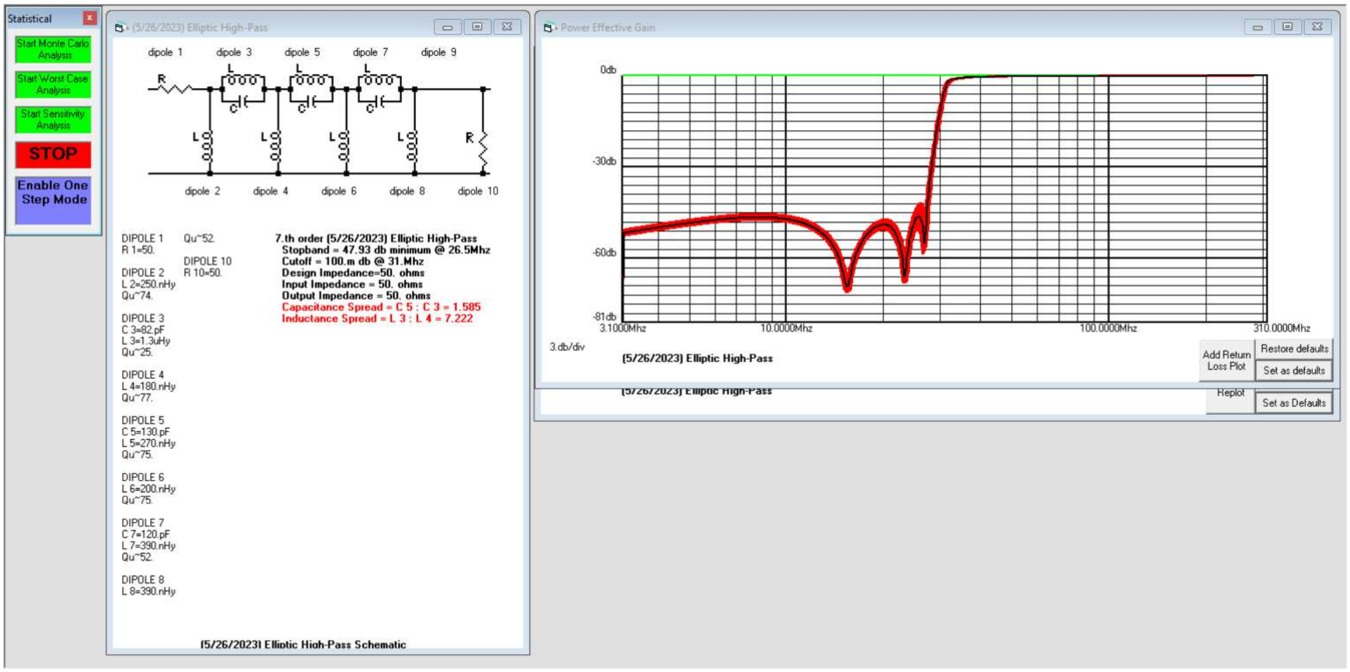
<u>30 MHz highpass filter</u>:
It is desirable to have 40 dB attenuation at the Citizen Band upper band edge of 27.410 MHz without too much loss above 30 MHz. These requirements indicate a relatively high order Chebyshev or Elliptic type. Of these, the Elliptic provides the best overall performance.

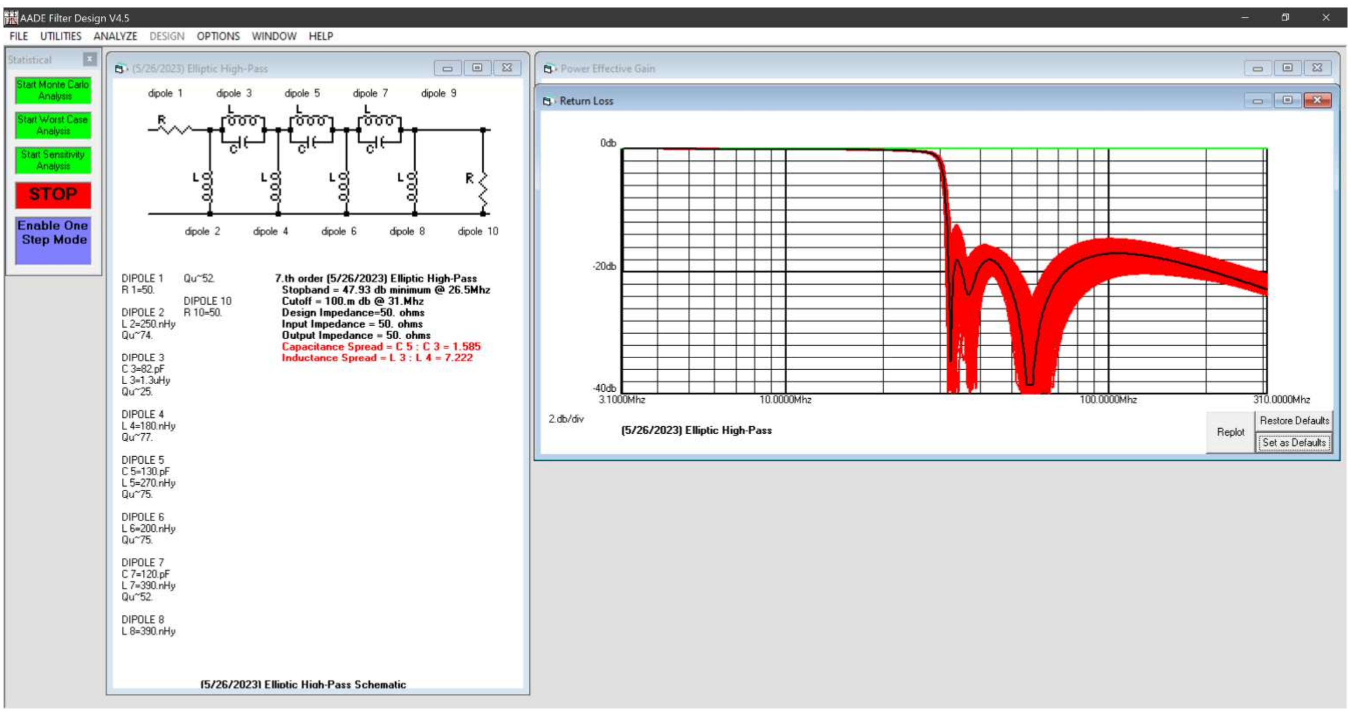
The 30 MHz highpass filter design criteria are:
Fc = 31 MHz with ≤ 0.1 dB ripple in the passband and at the cutoff frequency Fc
Fs = 26.5 MHz with ≥ 40 dB rejection in the stopband and at the stopband frequency Fs

The proposed 30 MHz filter is shown below with catalog component values. Also shown are the filter attenuation and return loss after Monte Carol statistical analysis.

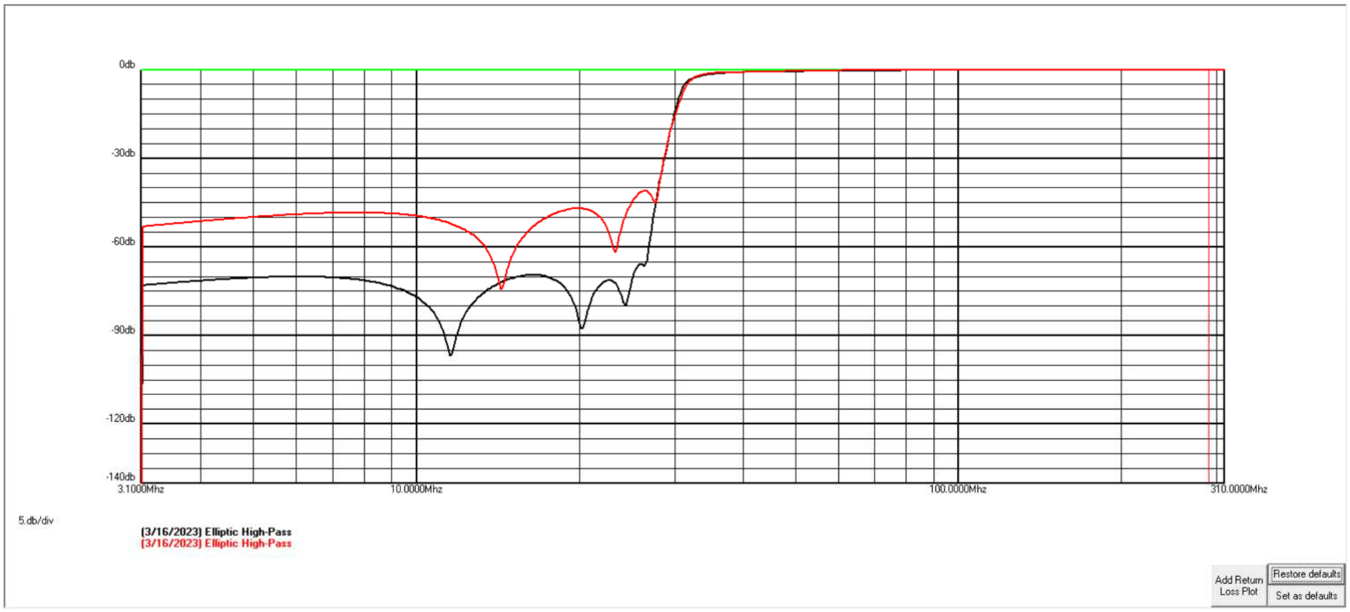
Characteristics of the final 30 MHz HPF from the simulation with single catalog component values:

- ✓ Type: Elliptic
- ✓ Order: 7
- ✓ Attenuation at 27.410 MHz: 41.5 dB
- ✓ Attenuation at 30.0 MHz: 11.5 dB
- ✓ Attenuation at 31.3 MHz: 3.0 dB
- ✓ Return loss at 31.0 MHz: 6.3 dB
- ✓ Minimum return loss above 31 MHz: 17.1 dB





Comparison of 30 MHz HPF 7th (red) and 9th (black) order Elliptic HPF for CBRS rejection:



6. ARX Rev. I Filters

The following sections describe the construction and measurements of prototype lowpass and highpass filters to be used in the Rev. I ARX. The filters are: 3 MHz HPF, 10 MHz HPF, 20 MHz HPF, 30 MHz HPF, 73.5 MHz LPF and 83.7 MHz LPF. All filters except the 83.7 MHz lowpass filter were synthesized and simulated with the AADE Filter Design tool as described in section 3. The 83.7 MHz filter is copied from the 83.7 MHz filter used in the Rev. H ARX. Several versions of the filters were designed and constructed. The filter simulations were compared to measurements with a Vector Network Analyzer.

All filter PCBs were designed as 4-layer boards with FR4 laminate. The Signal path traces are on the Top layer and the associated Return path traces are on the Inner Layer-1 (IN1). Vias interconnect the SMD ground pads on the Top Layer to IN1 and the Bottom Layer. The Inner Layer-2 (IN2) is not connected to the vias or anything else in the prototype filter PCBs. Stitching vias also connect the Top Layer to IN1 and the Bottom Layer. This stackup emulates the planned stackup for the final ARX PCBs in which IN2 will be used but not for the RF signal or return paths.

PCBs were procured from Galaxy and JLCPCB. The specified stackup was identical except for the materials used in the inner layers. The Galaxy order was supplied with 0.21 mm (8 mil) FR4 outer core layers and 1.02 mm (40 mil) inner core layer whereas JLCPCB was supplied with 0.21 mm (8 mil) prepreg inner layers and 1.07 mm FR4 inner core. In both cases, the copper was 1 oz on the outer layers and 0.5 oz on the inner layers.

Galaxy stackup total thickness 1.63 mm (64 mils) (upper) and JLCPCB stackup total thickness 1.59 mm (62.4 mils) (lower):

1		1 OZ PATT. PLATE	.0014
		1 OZ. COPPER	.0014
	FR4 0.008	.008 FR4 CORE	.008
2		1 OZ. COPPER	.0014
		1PC 1080 & 1PC 2113	*.0058*
	.028 FR4	***.028 FR4 UNCLAD***	*.028*
		1PC 1080 & 1PC 2113	*.0058*
3		1 OZ. COPPER	.0014
	FR4 0.008	.008 FR4 CORE	.008
4		1 OZ. COPPER	.0014
		1 OZ PATT. PLATE	.0014

2) JLC04161H-7628 Stackup

Layer	Material Type	Thickness	
Layer	Copper	0.035mm	
Prepreg	7628*1	0.2104mm	
inner Layer	Copper	0.0152mm	
Core>	Core	1.065mm	1.1mm (with copper core)
inner Layer	Copper	0.0152mm	
Prepreg	7628*1	0.2104mm	
Layer	Copper	0.035mm	

For reference, the stackup used with the Rev. G ARX PCBs is shown below.

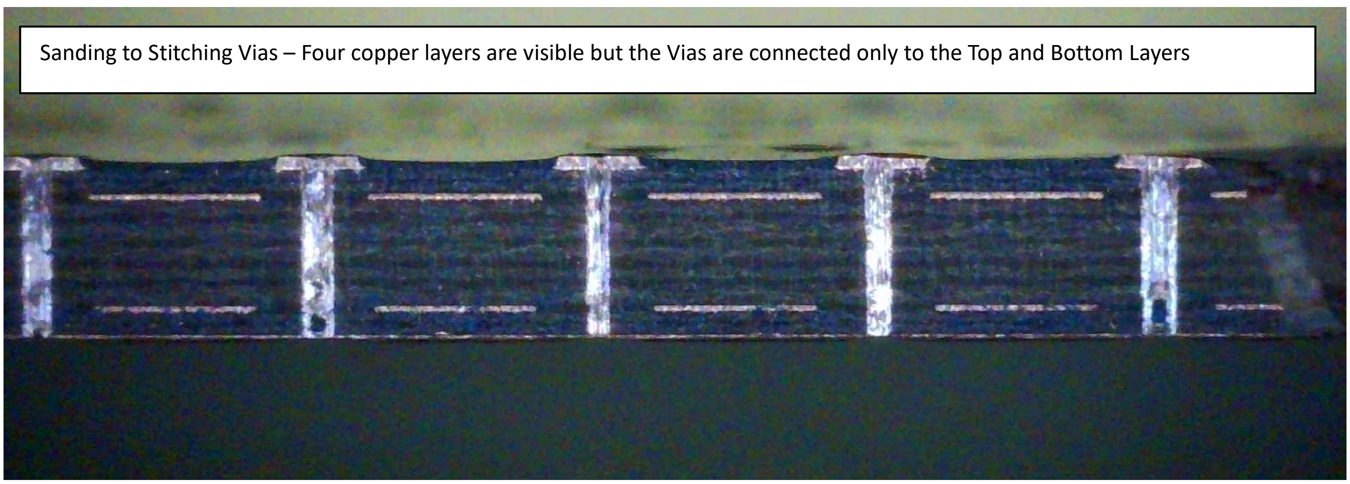
Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant	Pullback (mil)	Orientation	Coverlay Expansion
Top Overlay	Overlay							
Top Solder	Solder Mask/...	Surface Mat...	0.4	Solder Resist	3.5			0
Top Layer	Signal	Copper	1.4				Top	
Dielectric1	Dielectric	None	12.6	FR-4	4.8			
Mid-Layer 1	Signal	Copper	1.4				Not Allowed	
Dielectric2	Dielectric	None	12.6	FR-4	4.8			
Mid-Layer 2	Signal	Copper	1.4				Not Allowed	
Dielectric3	Dielectric	None	12.6	FR-4	4.8			
Bottom Layer	Signal	Copper	1.4				Bottom	
Bottom Solder	Solder Mask/...	Surface Mat...	0.4	Solder Resist	3.5			0
Bottom Over...	Overlay							

7. Comparison of *Universal Filter* PCB cross-sections used in the first phase of the evaluation:

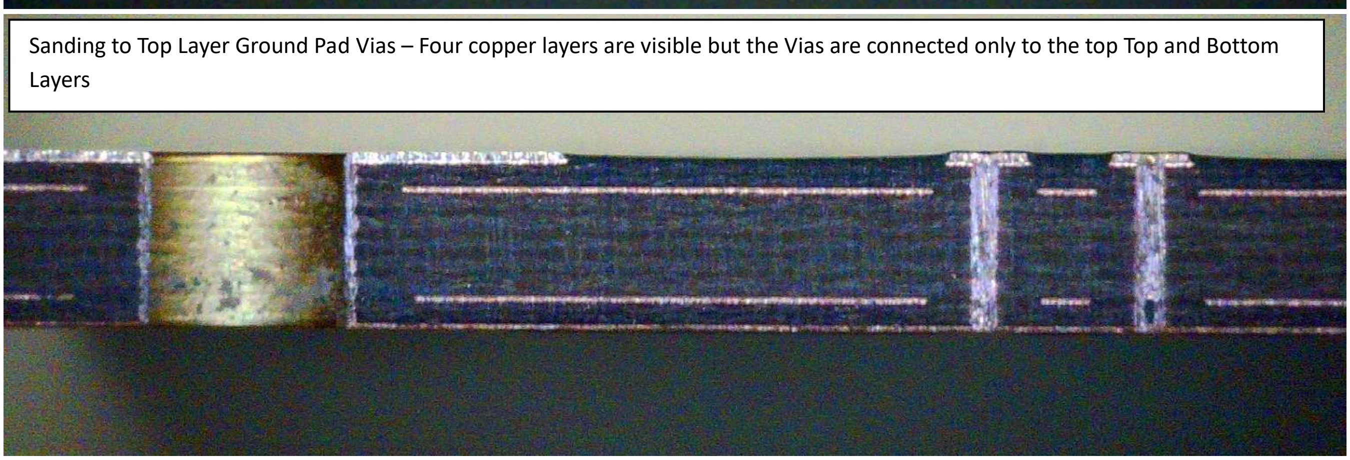
We attempted to design a *universal* printed circuit board that would allow construction of all types of relevant filter types including Butterworth, Chebyshev, Elliptic and others of order up to 7^{th} while allowing capacitors to be connected in parallel and inductors to be connected in series to enable fine tuning. This section describes that effort.

The first batch of the Universal Filter PCBs produced by Galaxy had the vias incorrectly connected from the Top Layer only to the Bottom Layer and not IN1. This was corrected in the second batch of PCBs produced by Galaxy. PCBs also were procured from JLCPCB and were correctly made. The PCB cross-sections were examined by sanding down one long edge until the Stitching vias and then the Grounding vias were exposed as shown below.

<u>Galaxy Original Filter PCBs: Top of PCB is up</u>

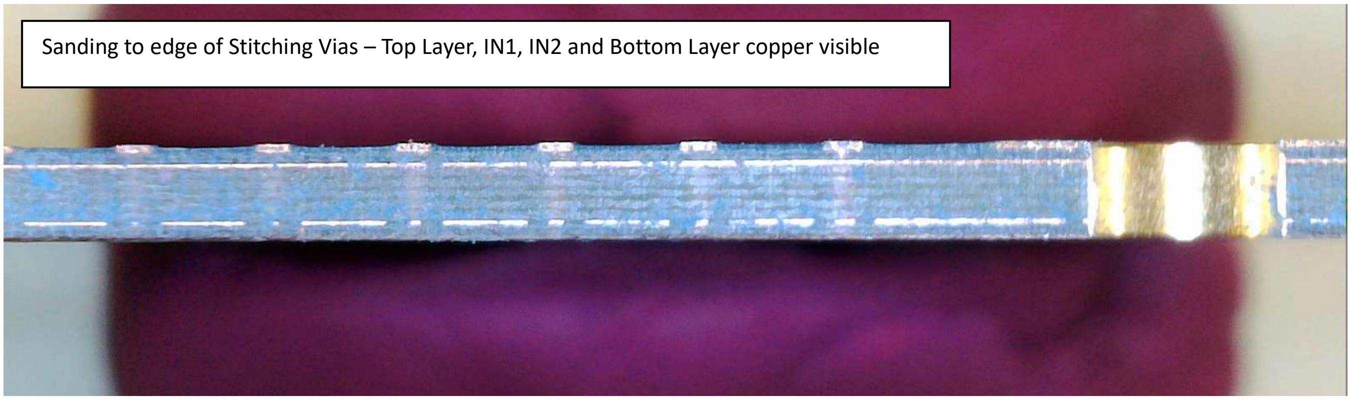


Sanding to Stitching Vias – Four copper layers are visible but the Vias are connected only to the Top and Bottom Layers

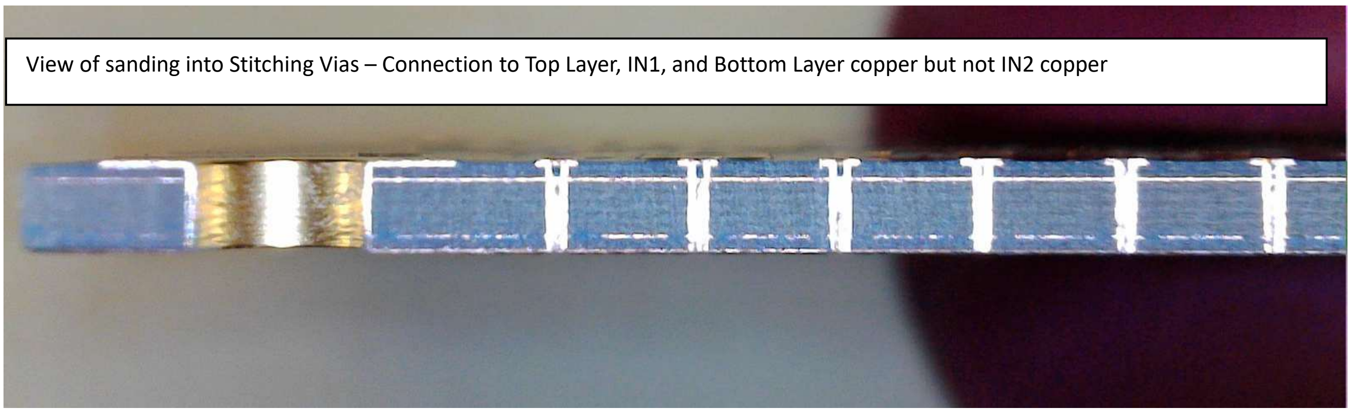


Sanding to Top Layer Ground Pad Vias – Four copper layers are visible but the Vias are connected only to the top Top and Bottom Layers

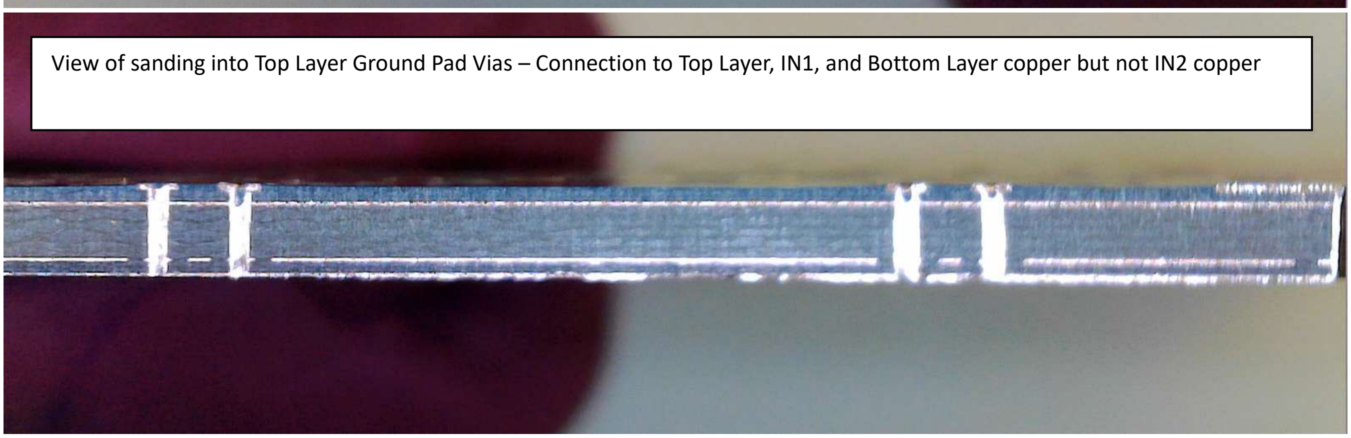
Galaxy Replacement Filter PCBs: Top of PCB is up



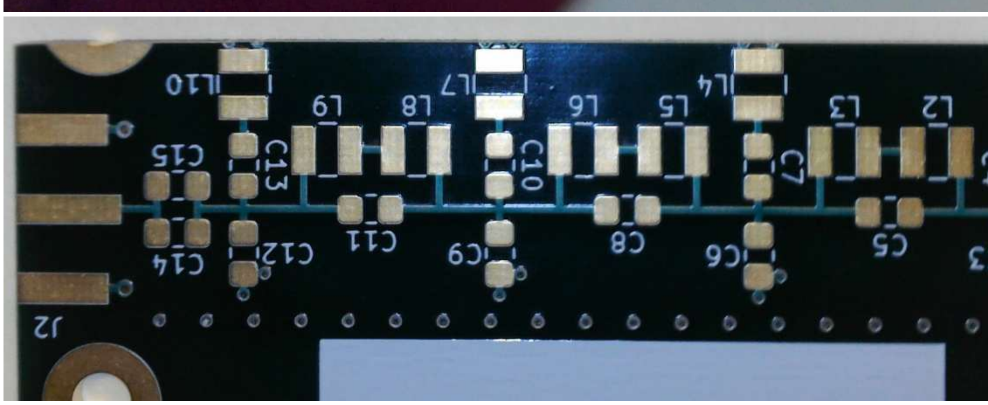
Sanding to edge of Stitching Vias – Top Layer, IN1, IN2 and Bottom Layer copper visible



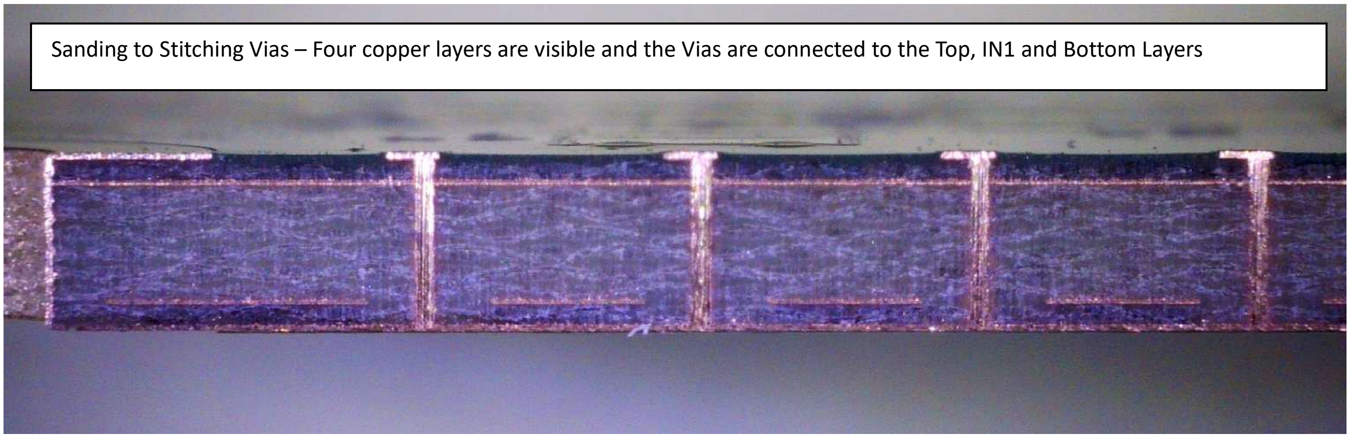
View of sanding into Stitching Vias – Connection to Top Layer, IN1, and Bottom Layer copper but not IN2 copper



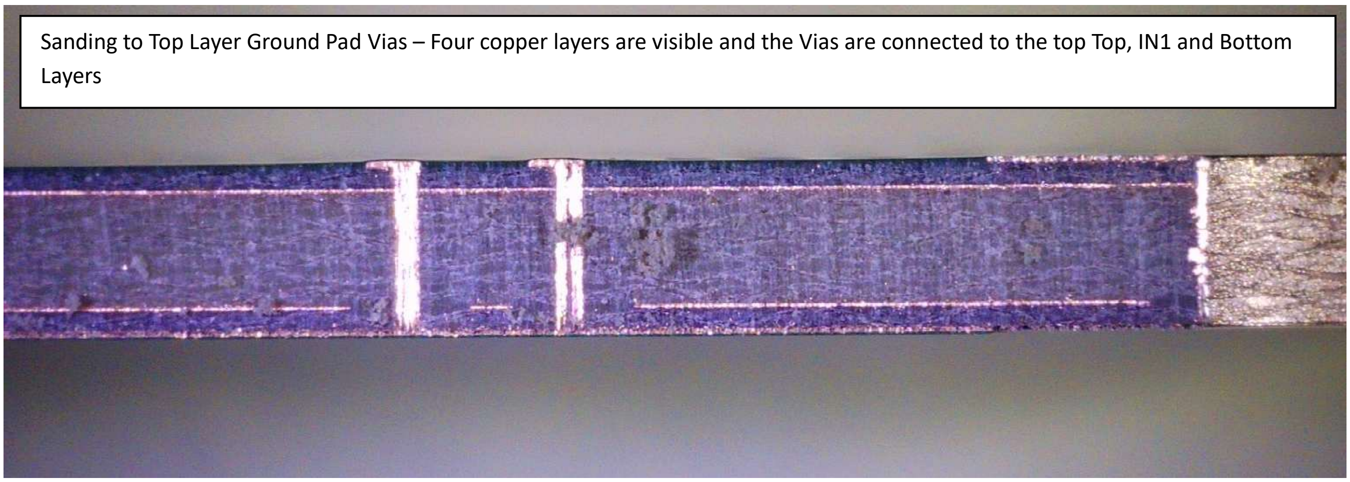
View of sanding into Top Layer Ground Pad Vias – Connection to Top Layer, IN1, and Bottom Layer copper but not IN2 copper



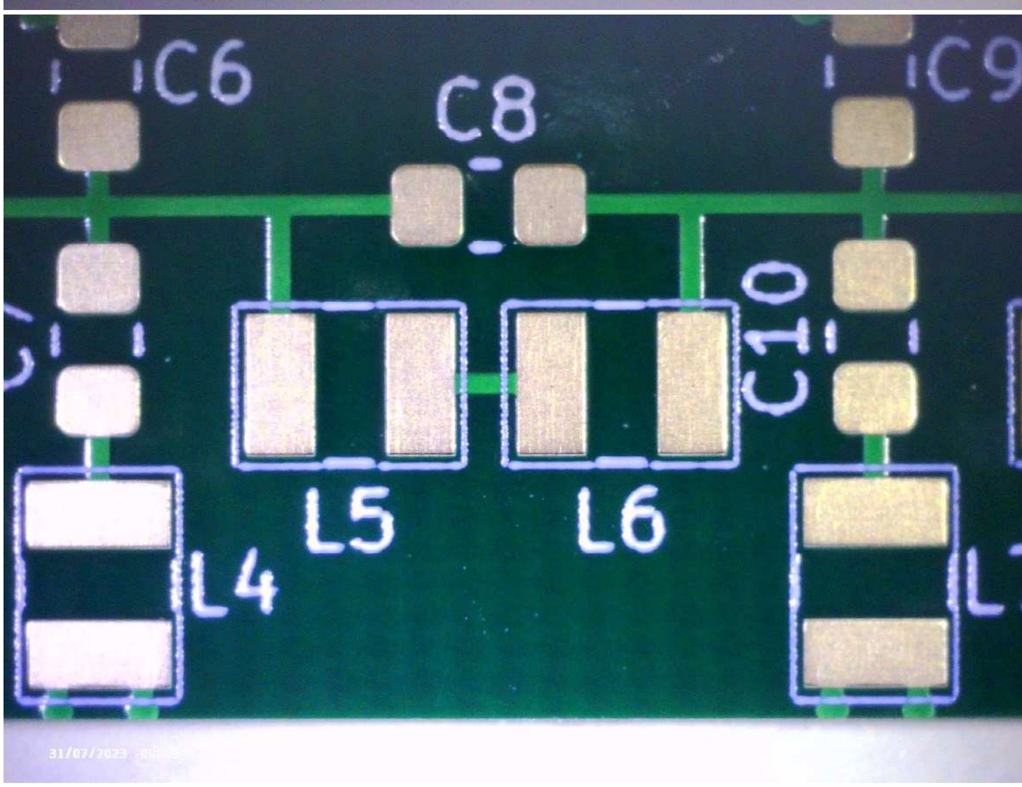
<u>JLCPCB No. 1 Filter PCBs: Top of PCB is up</u>



Sanding to Stitching Vias – Four copper layers are visible and the Vias are connected to the Top, IN1 and Bottom Layers



Sanding to Top Layer Ground Pad Vias – Four copper layers are visible and the Vias are connected to the top Top, IN1 and Bottom Layers



8. Filter Measurements & Simulation:

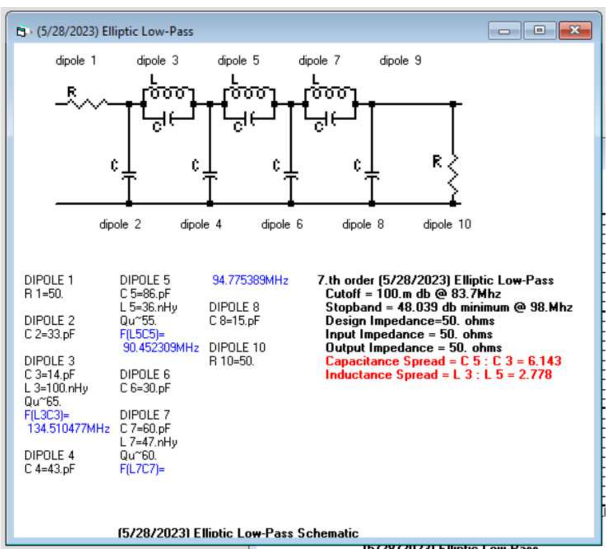
The filters on the Universal PCB did not perform as expected in the VHF range as shown by the representative measurements below. The measured insertion loss of the VHF lowpass filters far exceeded the simulated loss at the cutoff frequency and return losses at VHF were lower than expected.

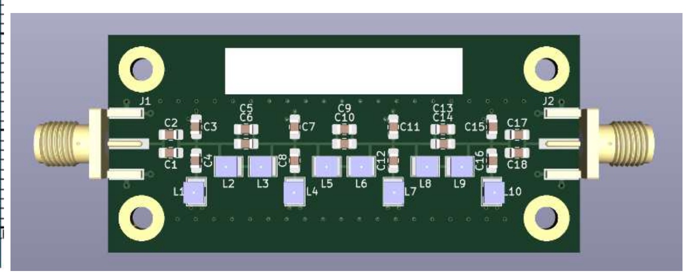
VHF-HI (83.7 MHz cutoff frequency):

Note: (LPF No1 is original Galaxy PCB and LPF No4 is replacement Galaxy PCB)

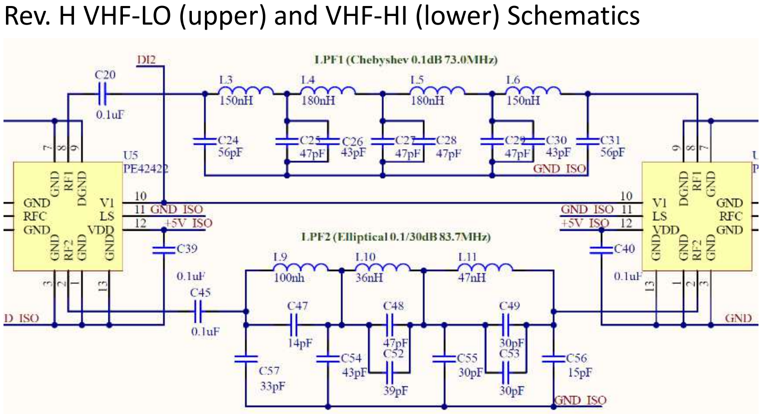
Freq (MHz)	LPF No1 – As Built Insertion Loss	LPF No4 – As Built Insertion Loss	LPF Simulation Insertion Loss	Remarks
MHz	dB	dB	dB	
3	0.11	0.11	0.01	
10	0.17	0.18	0.05	
30	0.42	0.44	0.19	
82.2	14.7	16.3	2.2	
83.7	23.8	26.1	2.8	
88.0	31.1	34.4	17.2	
198.6	29.8	31.4	29.8	
3 dB freq	77.4 MHz	77.0 MHz	84.1 MHz	

LPF Simulation Schematic of the VHF-HI (83.7 MHz) LPF alongside a Gerber Viewer image of the Universal PCB



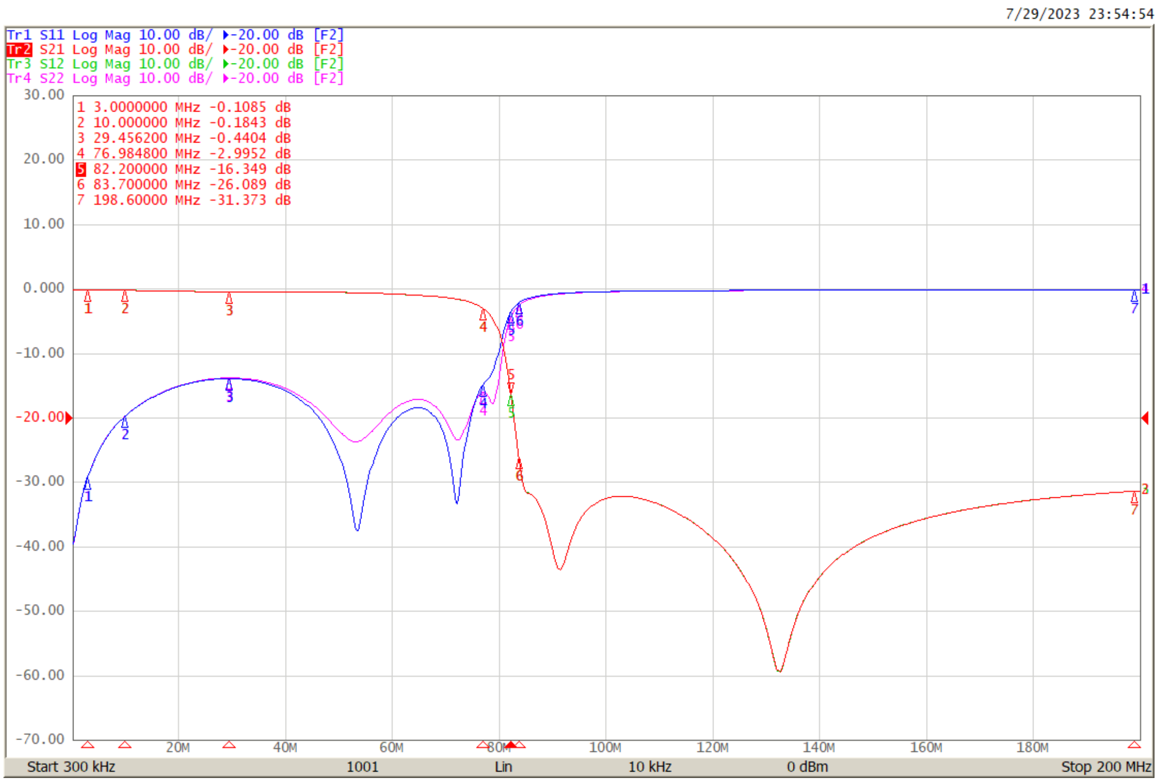


Rev. H VHF-LO (upper) and VHF-HI (lower) Schematics



VHF-HI No1 VNA Plot (Original Galaxy PCB):

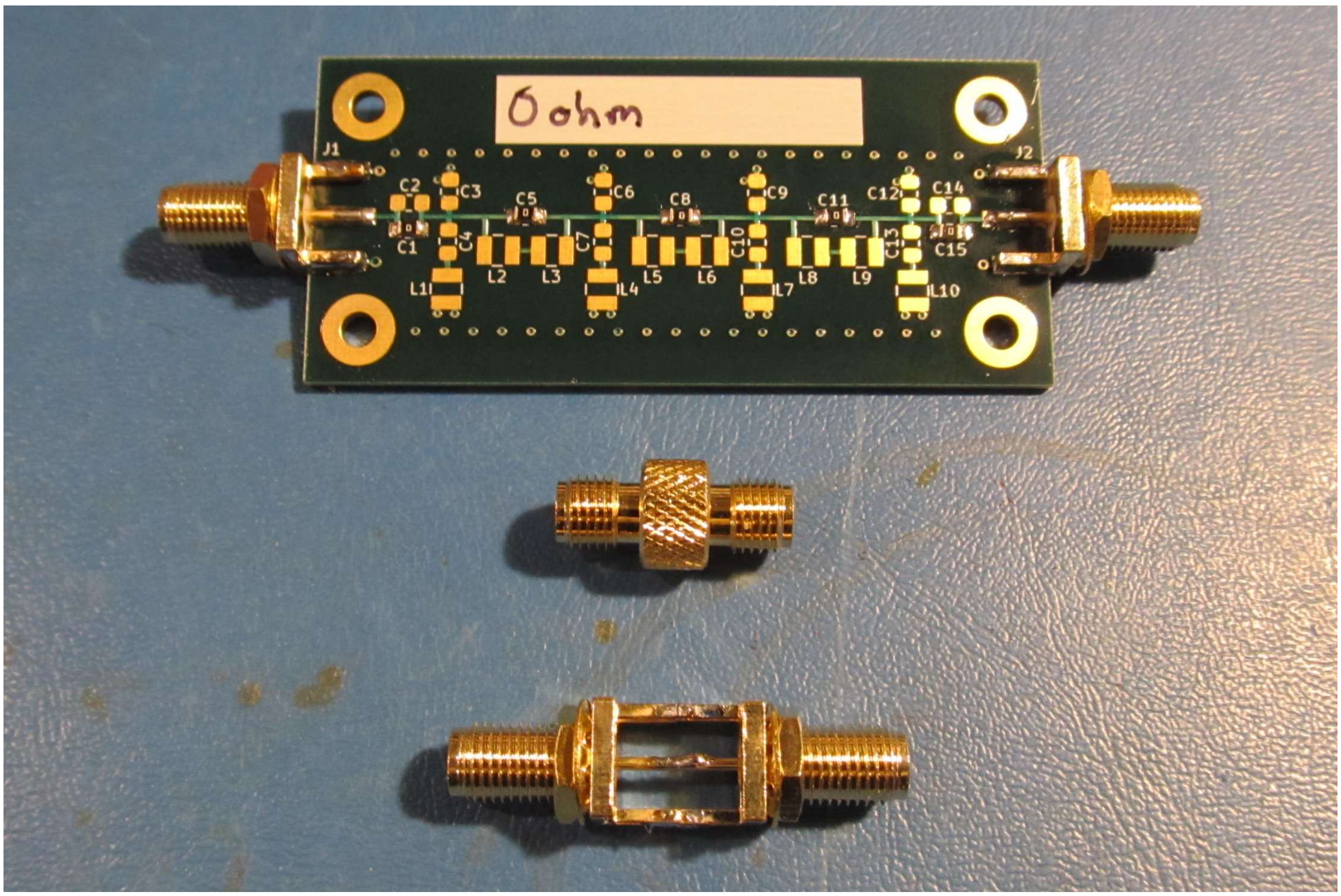
VHF-HI No4 VNA Plot (Replacement Galaxy PCB):



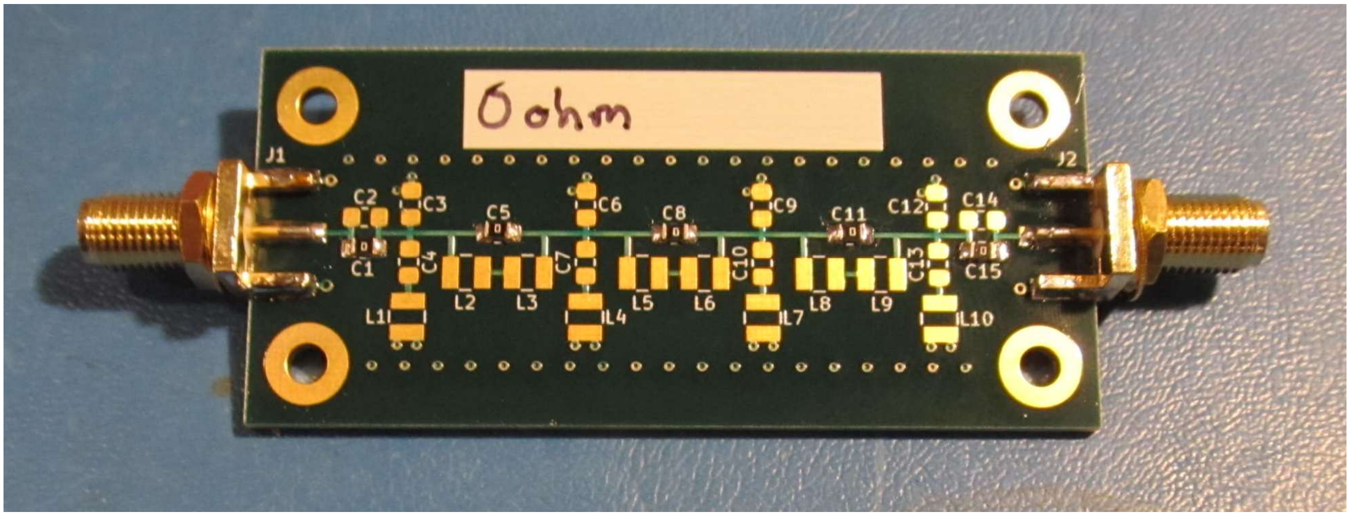
To troubleshoot the measured response problems, the Universal Filter PCBs were equipped only with 0 ohm resistors in the RF path; no reactive components were installed. The transmission and reflection coefficients were then measured with a VNA and compared to the same measurements for a coaxial coupler and back-to-back edge connectors as shown below.

☐ Galaxy Replacement PCB with 0 Ohm Resistors in C1, C5, C8, C11 and C15
☐ SMA-F : SMA-F Coupler (inexpensive type bought through Aliexpress)
☐ Back-to-Back SMA-F PCB Edge Connectors (inexpensive types bought through Aliexpress)

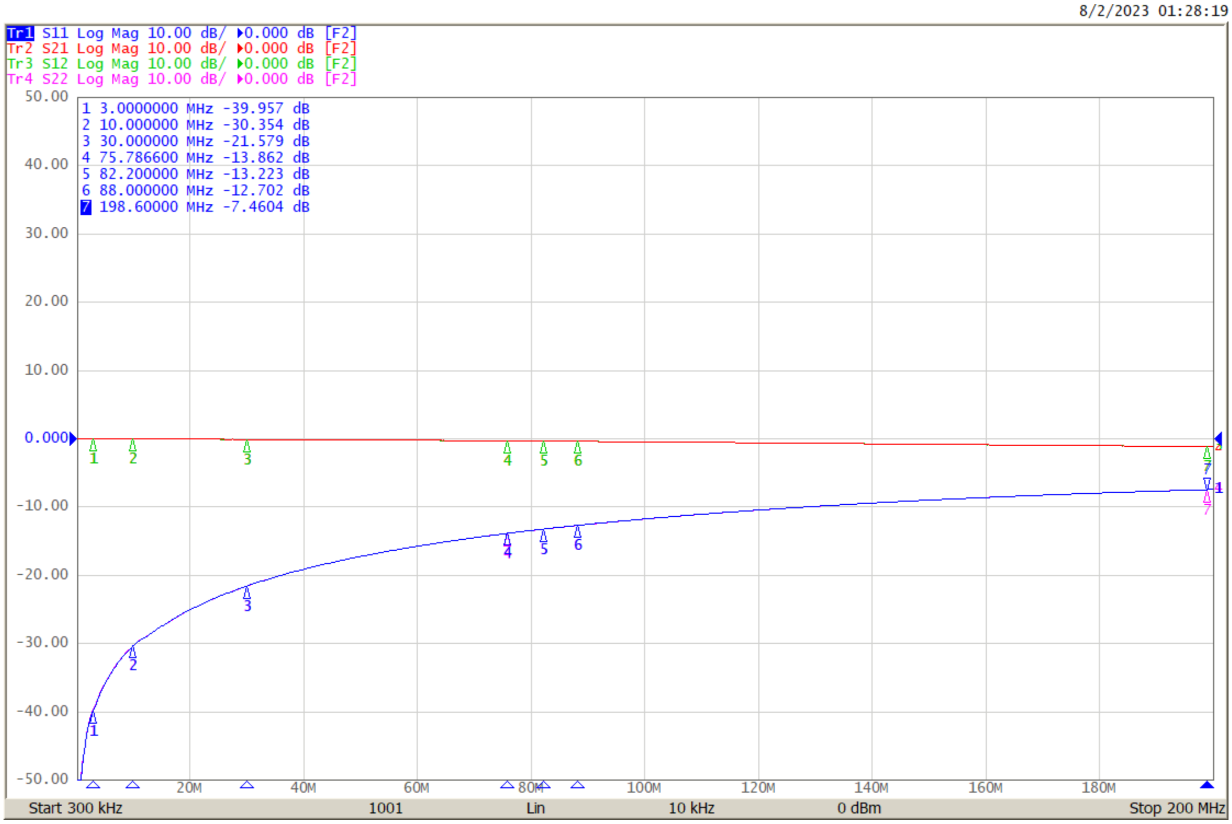
Image of devices used in the following measurements:



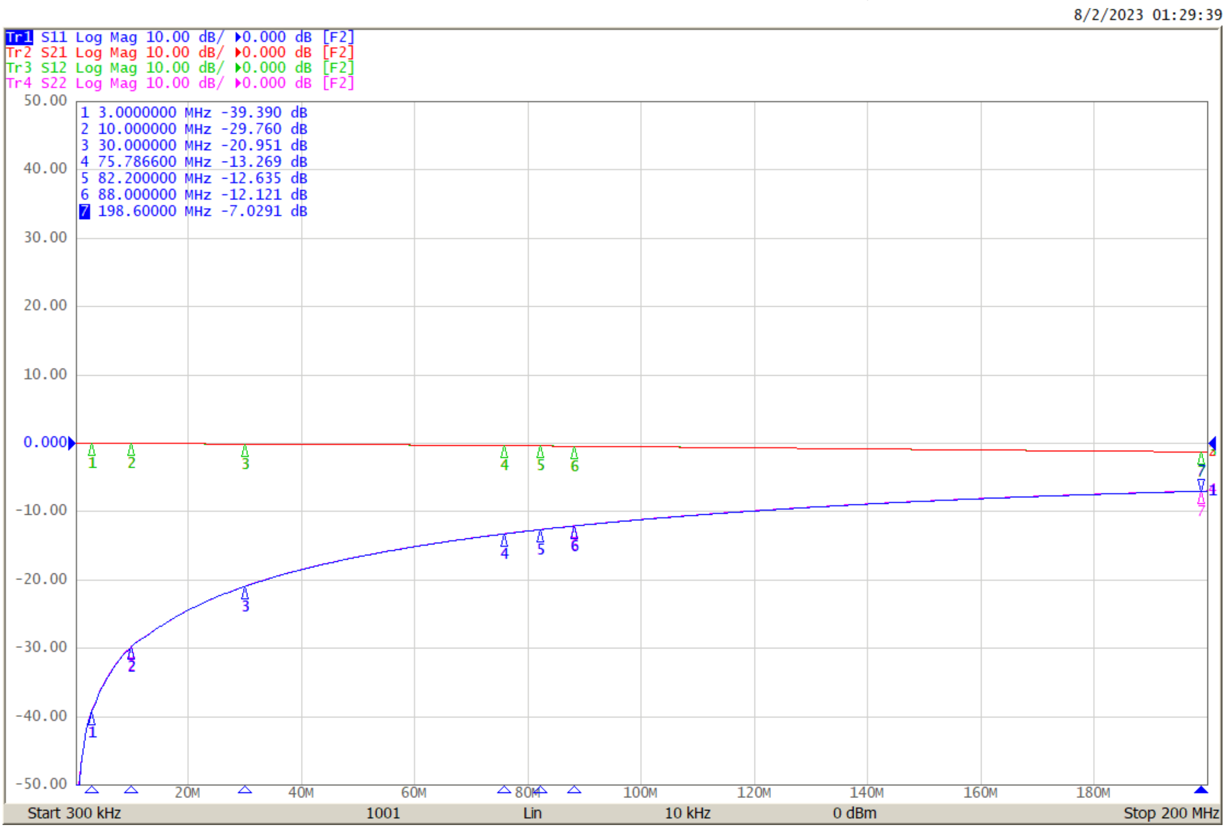
Typical PCB with 0 Ohm Resistors in C1, C5, C8, C11 and C15:



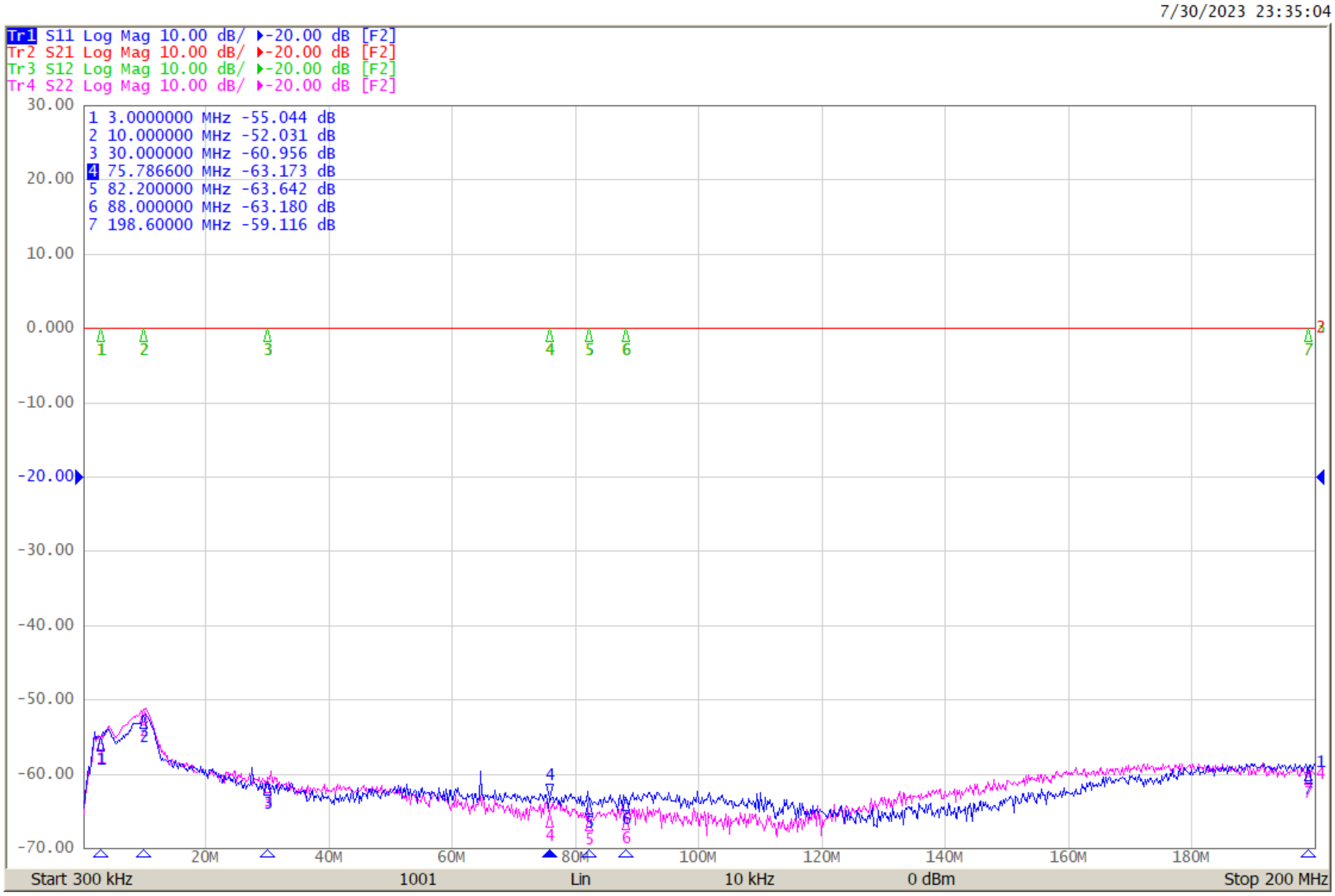
Galaxy Replacement PCB with 0 Ohm Resistors in C1, C5, C8, C11 and C15. Note poor return loss at 100 MHz:



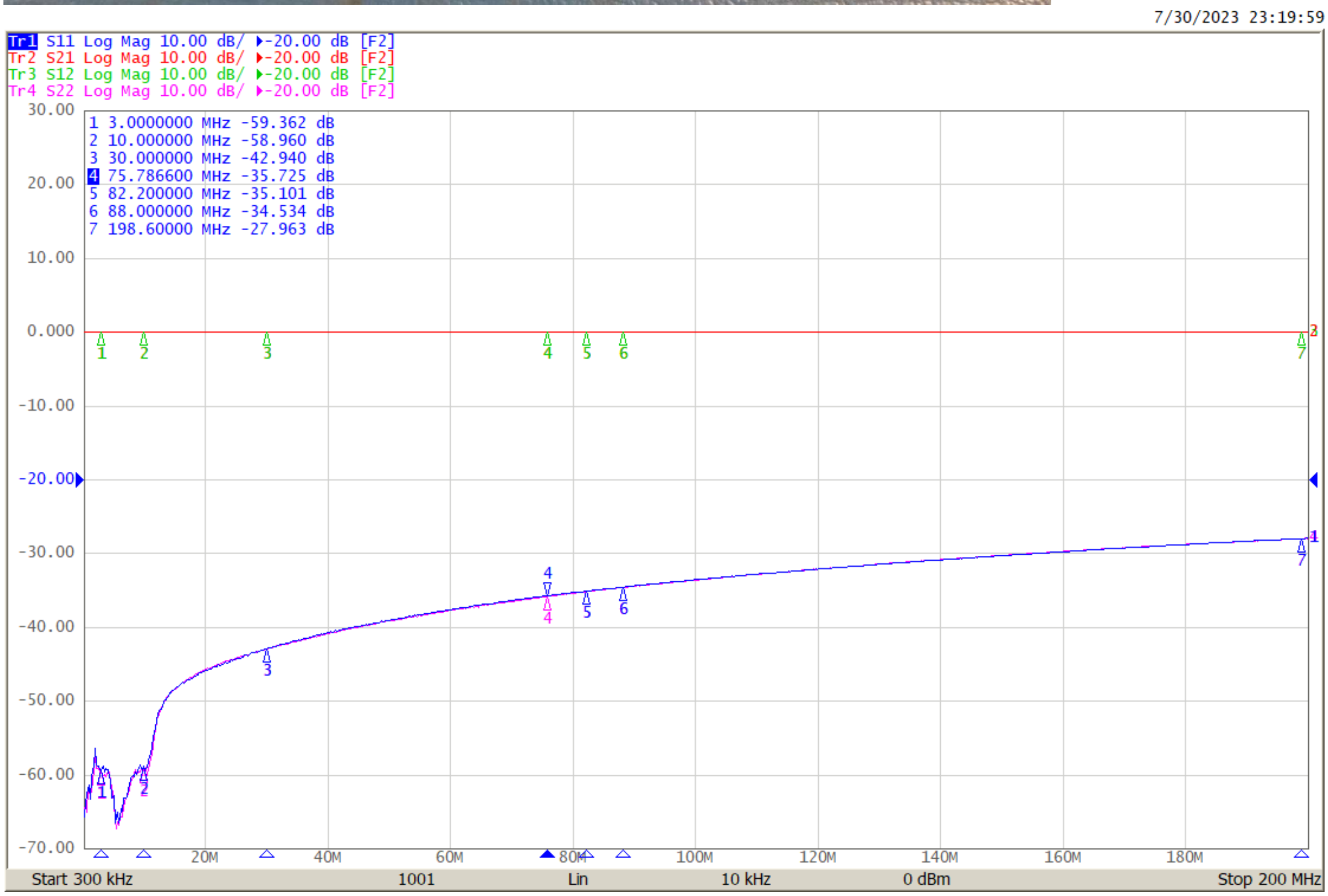
JLCPCB No. 1 PCB with 0 Ohm Resistors in C1, C5, C8, C11 and C15. Note poor return loss at 100 MHz:



SMA-F : SMA-F Coupler:



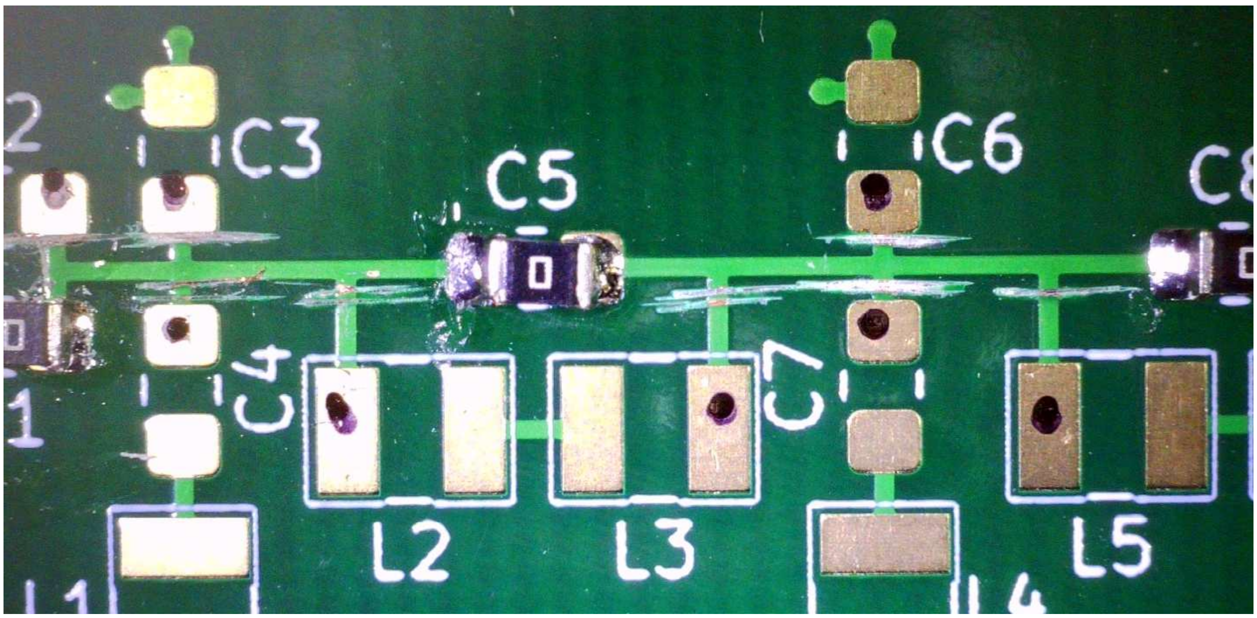
Back-to-Back SMA-F PCB Edge Connectors:



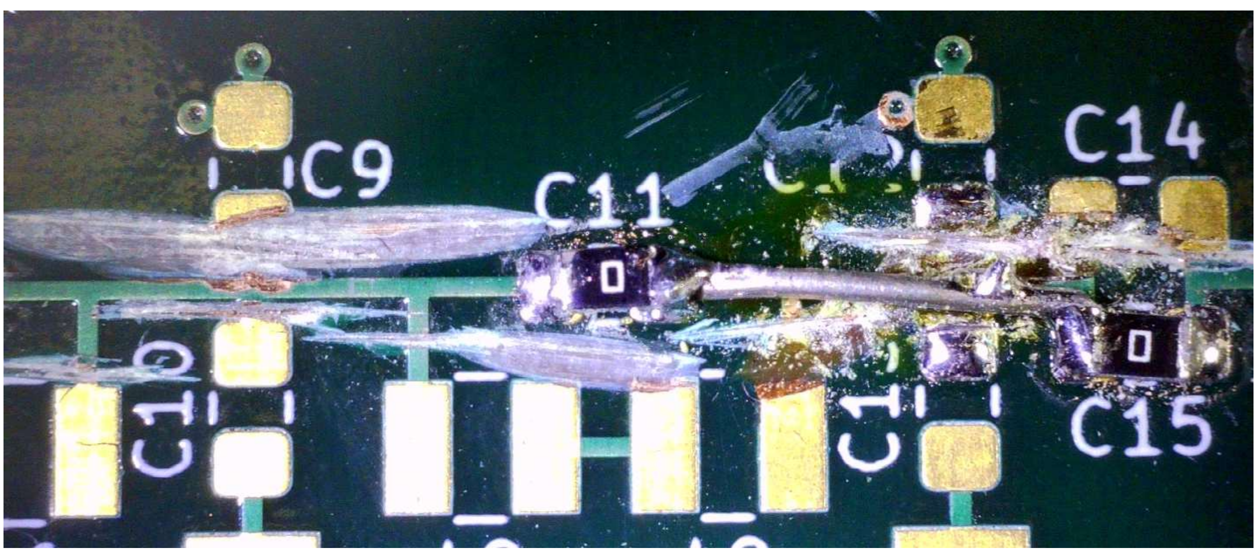
9. Comparison of PCBs with all unused pads cut out:

The above measurements revealed that the PCBs likely caused the incorrect responses. Based on a paper by Ed Troy of Aerospace Consulting LLC [https://rfandmicrowavedesign.com/assets/debug-lc-filter.pdf] that describes calculations of SMD pad capacitances and their effects on filter response characteristics, the traces to all unused pads on the Universal Filter PCB were cut and the boards with 0 ohm resistors were remeasured. Cutting out the unused pads improved the return loss by almost 10 dB at 100 MHz, indicating that our attempt to produce a universal prototype PCB would not support filters covering the VHF range.

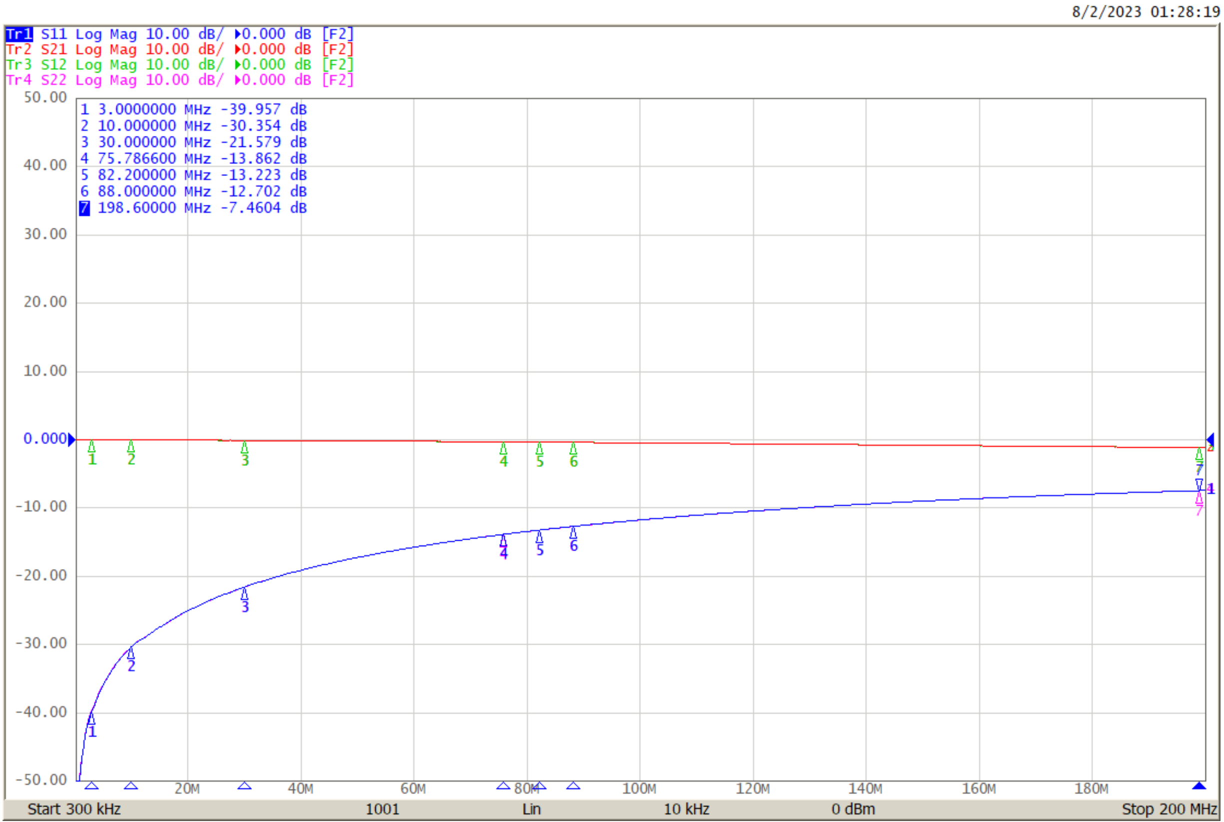
Exacto hobby knife: The black dots on the pads indicate that an ohmmeter was used to verify the open circuit from the pad to the center RF path trace. Note that a 0 ohm resistor can be seen in place of capacitor C5.



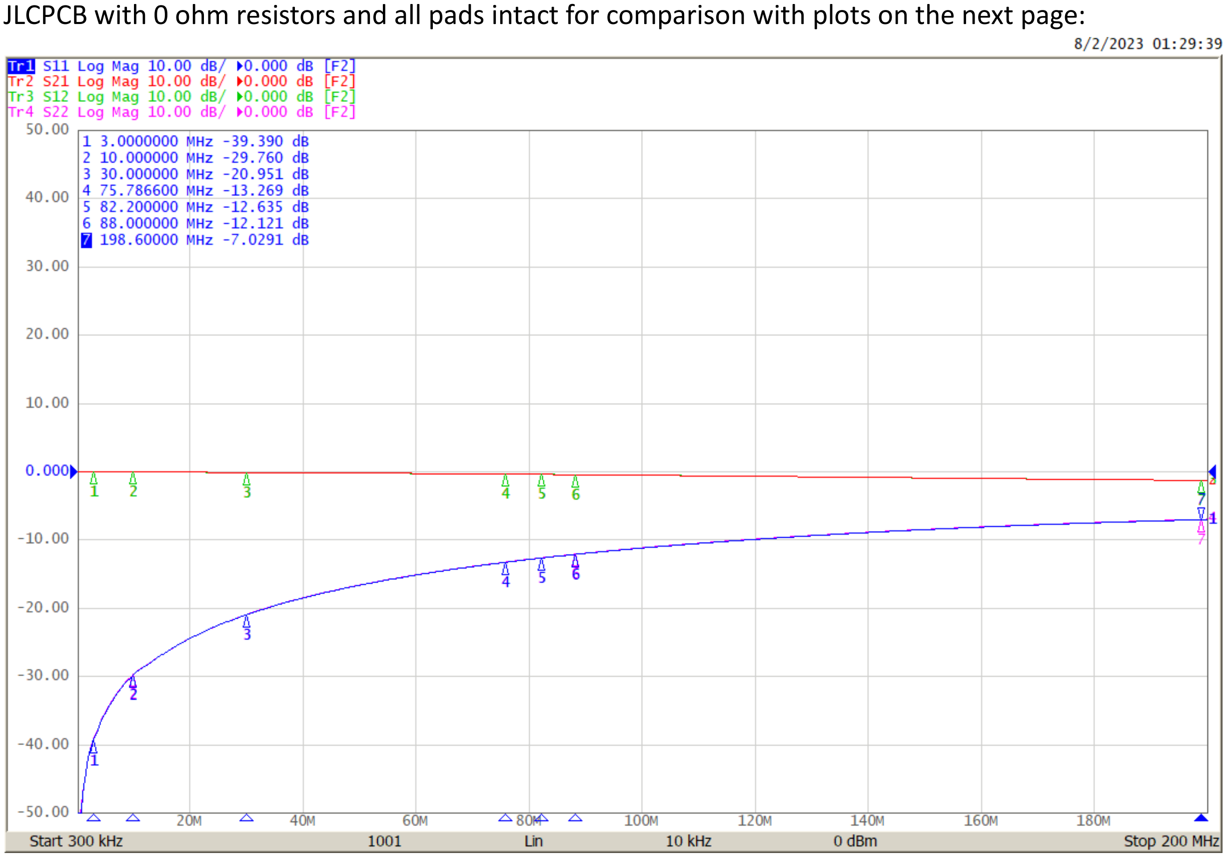
Dremel cutter: Too hard to control and did not work as expected.



Galaxy PCB with 0 ohm resistors and all pads intact for comparison with the plots on the next page:

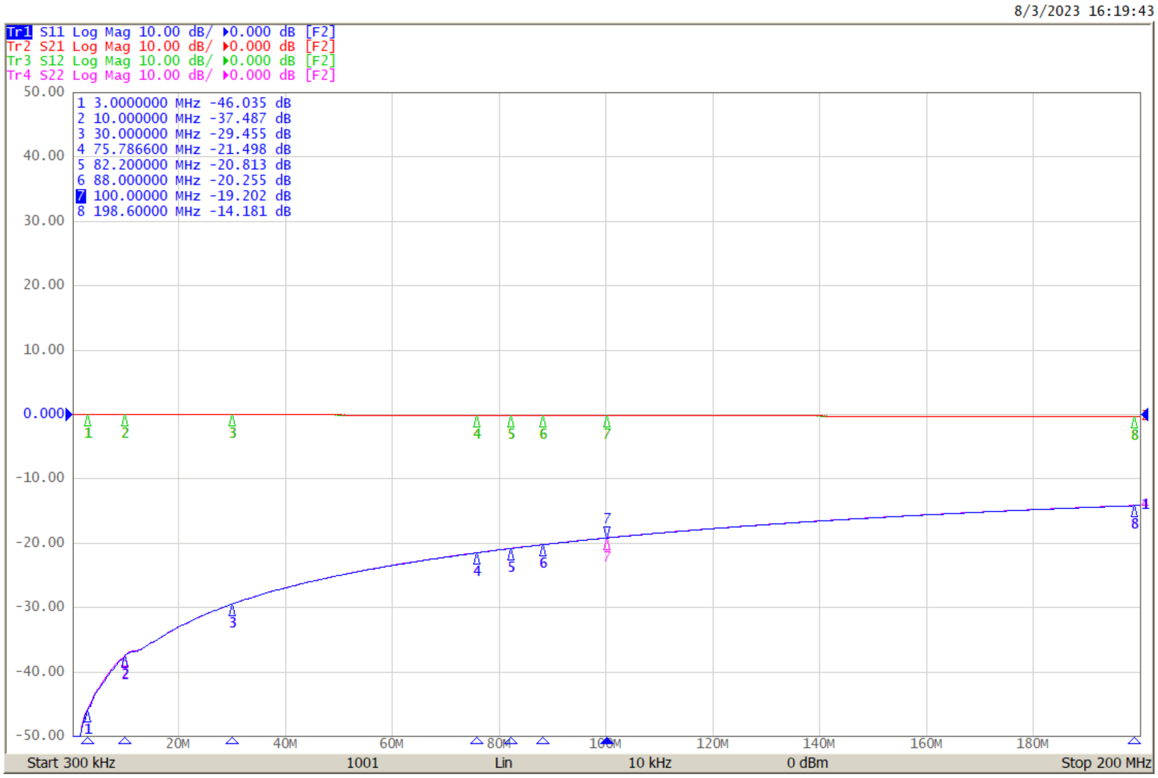


JLCPCB with 0 ohm resistors and all pads intact for comparison with plots on the next page:

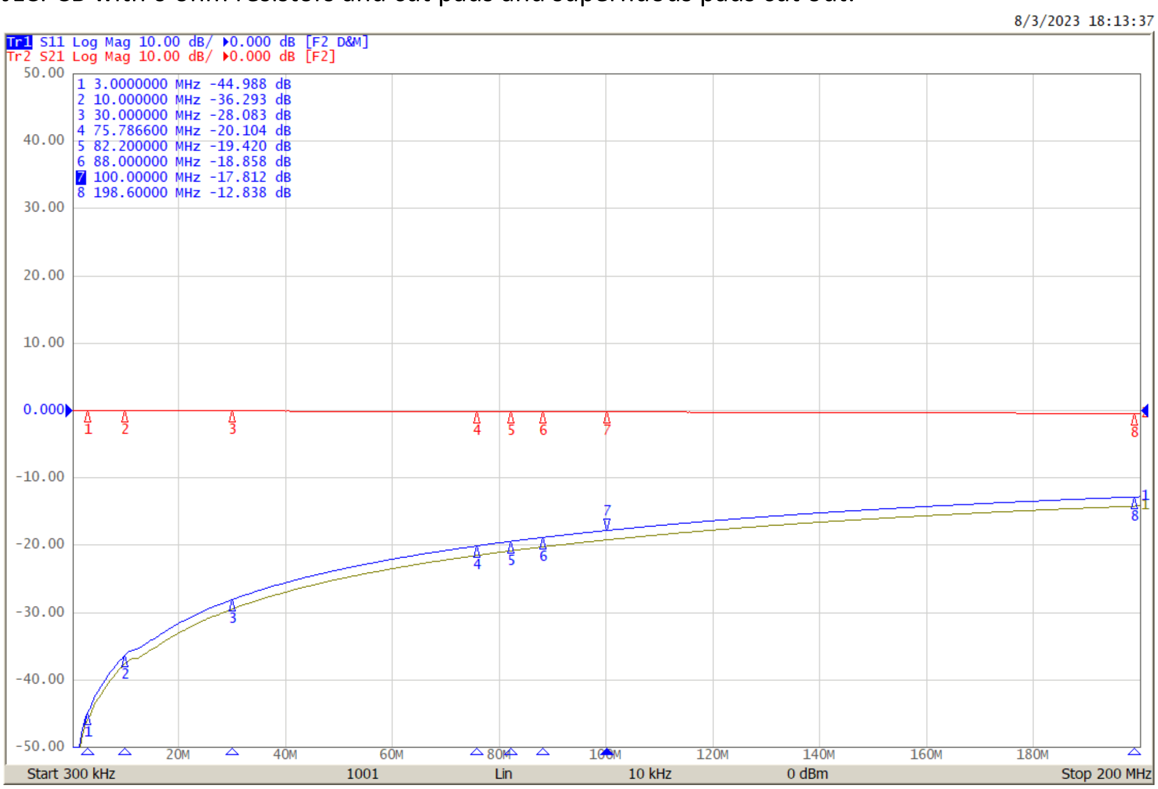


Galaxy PCB with 0 ohm resistors and superfluous pads cut out:

Note improvement in return loss at 100 MHz compared to the intact boards on the previous page



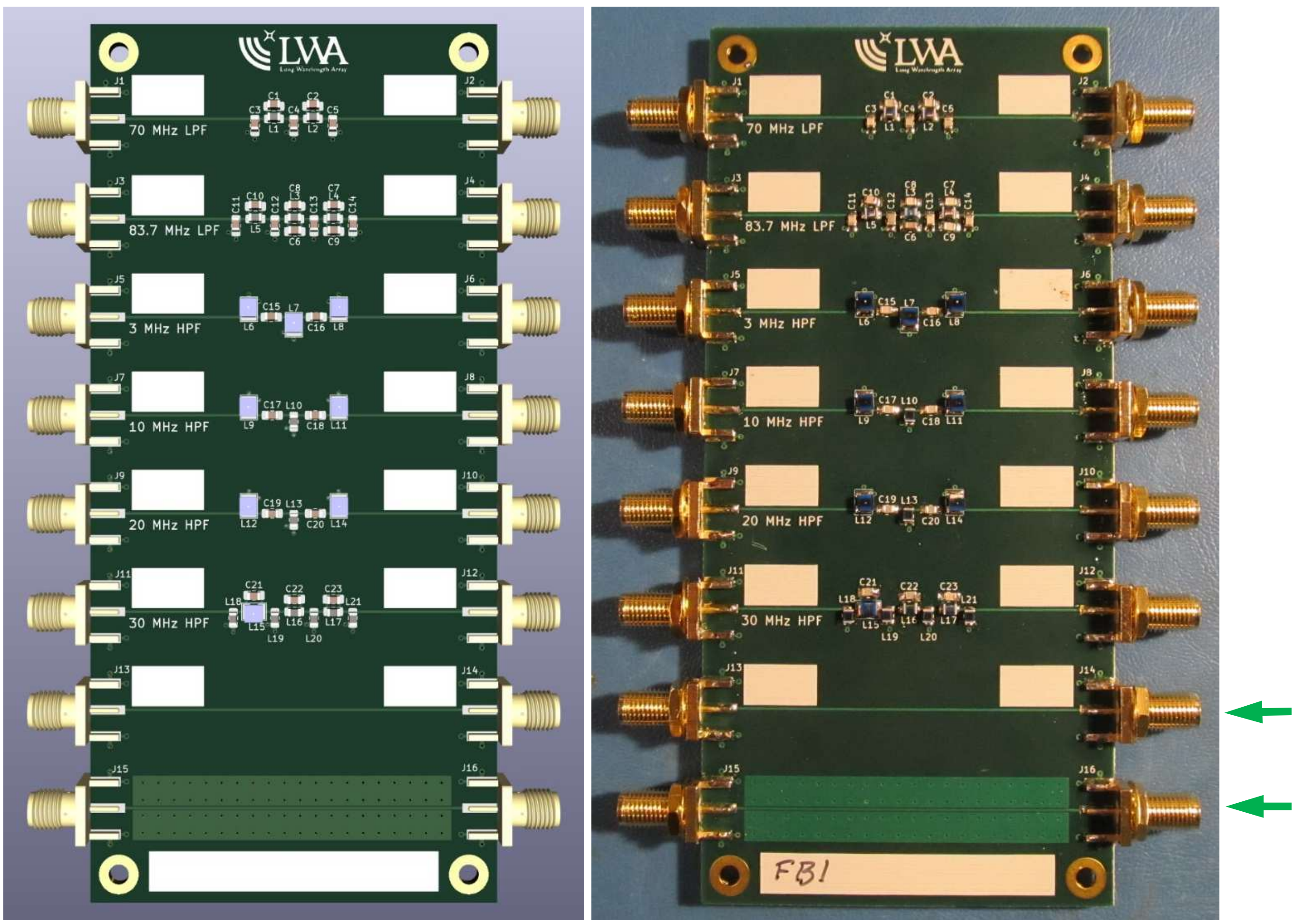
JLCPCB with 0 ohm resistors and cut pads and superfluous pads cut out:



10. All-In-One Filter PCB:

Because of its poor performance, the Universal Filter PCB concept described above was abandoned, and the prototype filter PCBs were then redesigned. The layouts of the six filters were based on the specific components used in each filter and no unnecessary pads or traces were placed. Also, the component spacings were tightened up to reduce trace inductance. All six filters were placed on one PCB, referred to herein as the *All-In-One Filter* PCB, along with Microstrip and Coplanar Waveguide traces for comparison with previous measurements. The PCB stackup and via connections between the layers of the All-In-One Filter PCB are identical to the Universal Filter PCB.

Gerber Viewer image (left) and actual filter PCB (right) of the All-In-One Filter PCB with Microstrip (upper arrow at lower right) and Coplanar Waveguide Traces (lower arrow) for investigation of PCB transmission properties and comparison:

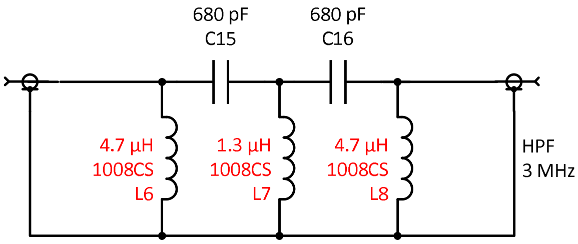


The original 5th order Elliptic 70 MHz LPF was later deemed inadequate in terms of insertion loss at 88 MHz and minimum return loss in the passband, so it was redesigned as a 7th order Elliptic 73.5 MHz LPF. Rather than produce another run of PCBs, the new filter was built on the existing All-In-One PCBs in the position for the 7th order 83.7 MHz filter (2nd filter from the top). The measurements below are for the new filter.

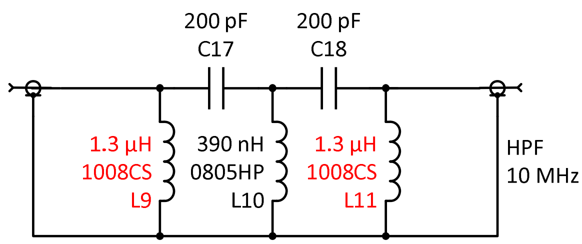
11. Filter Schematics:

The schematics below are of the filters to be used in the Rev. I ARX and show the actual component catalog values and the Coilcraft inductor series used in the designs and constructions of the prototype filters. All capacitors and inductors have ±2% tolerance. Capacitors are from various name brand manufacturers (Vishay, Kemet, Kyocera, Yageo, and Walsin) in size 0805 and C0G (NP0) dielectric. All inductors are ceramic core chip inductors from Coilcraft.

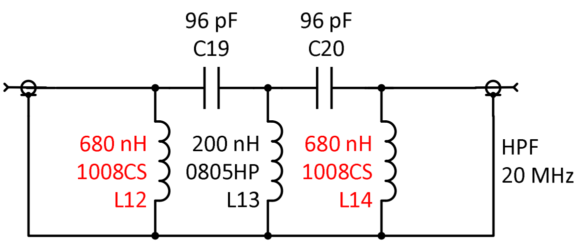
3 MHz Highpass Filter



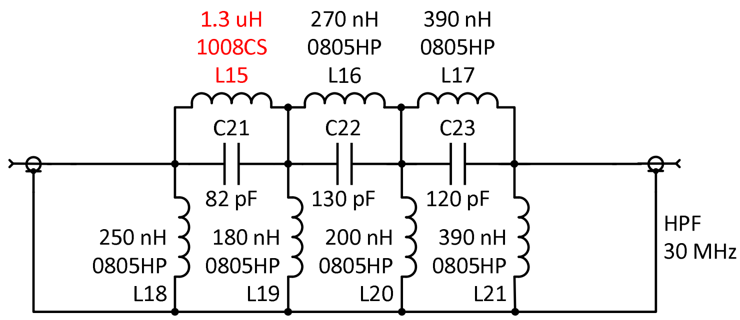
10 MHz Highpass Filter



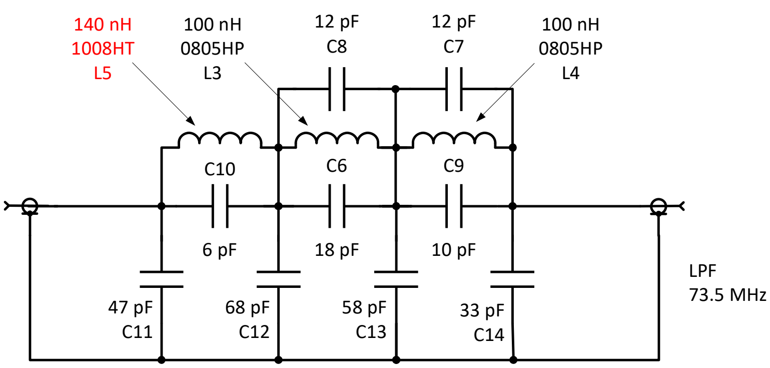
20 MHz Highpass Filter



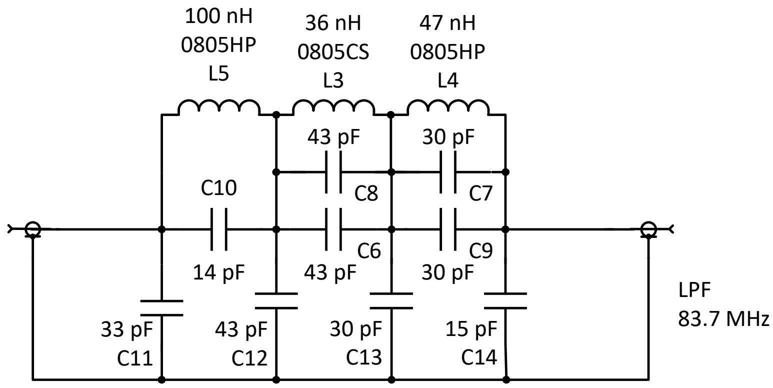
30 MHz Highpass Filter



73.5 MHz Lowpass Filter



83.7 MHz Lowpass Filter



12. Prototype Filter Measurements:

Summary of prototype filter characteristics and measurements:

3 MHz highpass filter Butterworth, 5th order Simulation: Fc = 3.0 MHz, Simulated = 3.8 dB; Measured = 4.5 dB Fs = 1.8 MHz, Simulated = 21.5 dB; Measured = 27.7 dB	10 MHz highpass filter Butterworth, 5th order Simulation: Fc = 10.0 MHz, Simulated = 3.6 dB, Measured = 3.8 dB Fs = 6.0 MHz, Simulated = 22.5 dB, Measured = 22.8 dB
20 MHz highpass filter Butterworth, 5th order Fc = 20 MHz, Simulated = 3.8 dB; Measured = 3.8 dB Fs = 12 MHz, Simulated = 22.6 dB; Measured = 23.0 dB	30 MHz highpass filter (design Fc = 26.5 MHz) Elliptic, 7th order Fc = 31.0 MHz, Simulated = 4.2 dB; Measured = 6.6 dB Fs = 27.41 MHz, Simulated = 41.5 dB; Measured = 43.1 dB
73.5 MHz lowpass filter Elliptic, 7th order Fc = 70 MHz, Simulated = 1.0 dB; Measured = 1.8 dB Fs = 88 MHz, Simulated = 40.0 dB; Measured = 39.1 Simulated minimum attenuation 88 to 108 MHz = 29.8 dB Measured minimum attenuation 88 to 108 MHz = 41.0 dB	83.7 MHz lowpass filter Elliptic, 7th order Fc = 82.2 MHz, Simulated = 2.1 dB; Measured = 3.4 dB Fs = 88 MHz, Simulated = 17.5 dB; Measured = 24.5 dB Simulated minimum attenuation 88 to 108 MHz = 15.2 dB Measured minimum attenuation 88 to 108 MHz = 24.5 dB

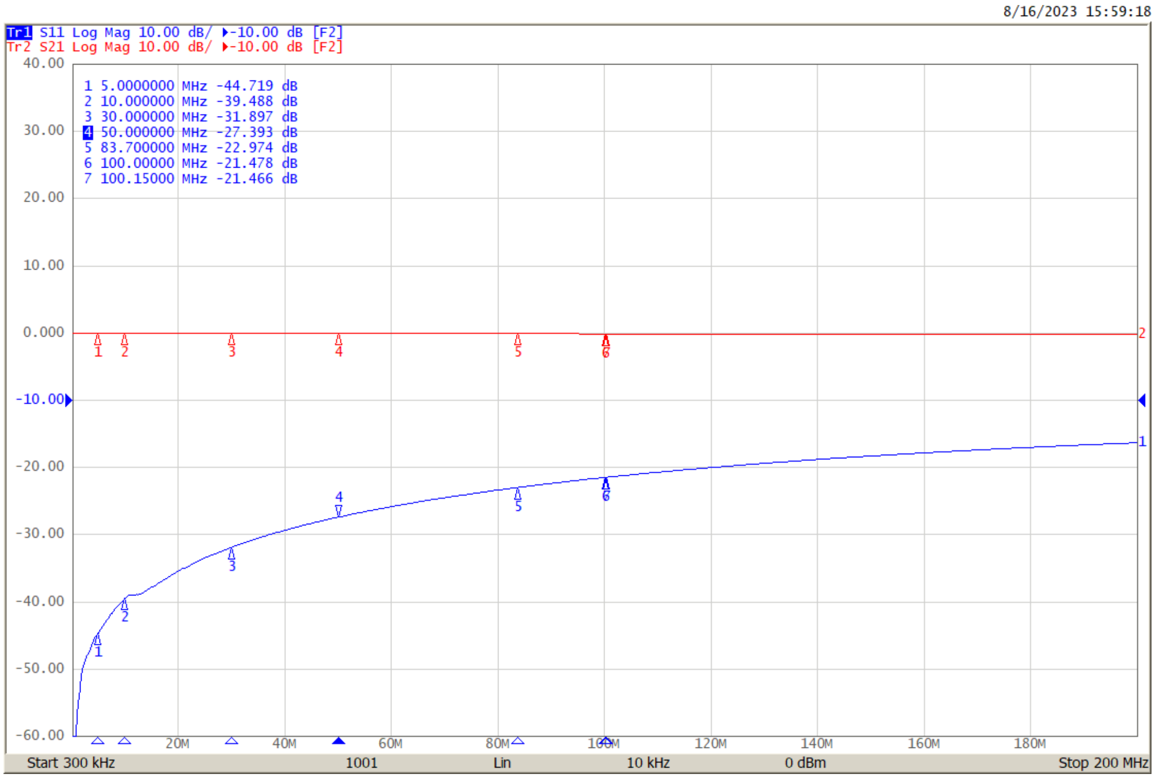
In addition to the filters, the Microstrip and Coplanar Waveguide transmission lines were measured and plotted as shown on the next page for reference. Note that the Microstrip is roughly equivalent to the previous measurements of the Universal Filter PCB with 0 ohm RF path resistors and the unused traces and SMD pads cutout.

The filter plots follow the Microstrip and Coplanar Waveguide plots. The individual filter S2P measurements and plots were made with a Copper Mountain Technologies M5045 Vector Network Analyzer; the M5045 plot for only one filter of each type is shown in this document. Also included are combined plots for three filters of each type. For the combination plots, the S2P data for the three filters from the M5045 measurements were imported into the DG8SAQ Vector Network Analyzer Software for plotting.

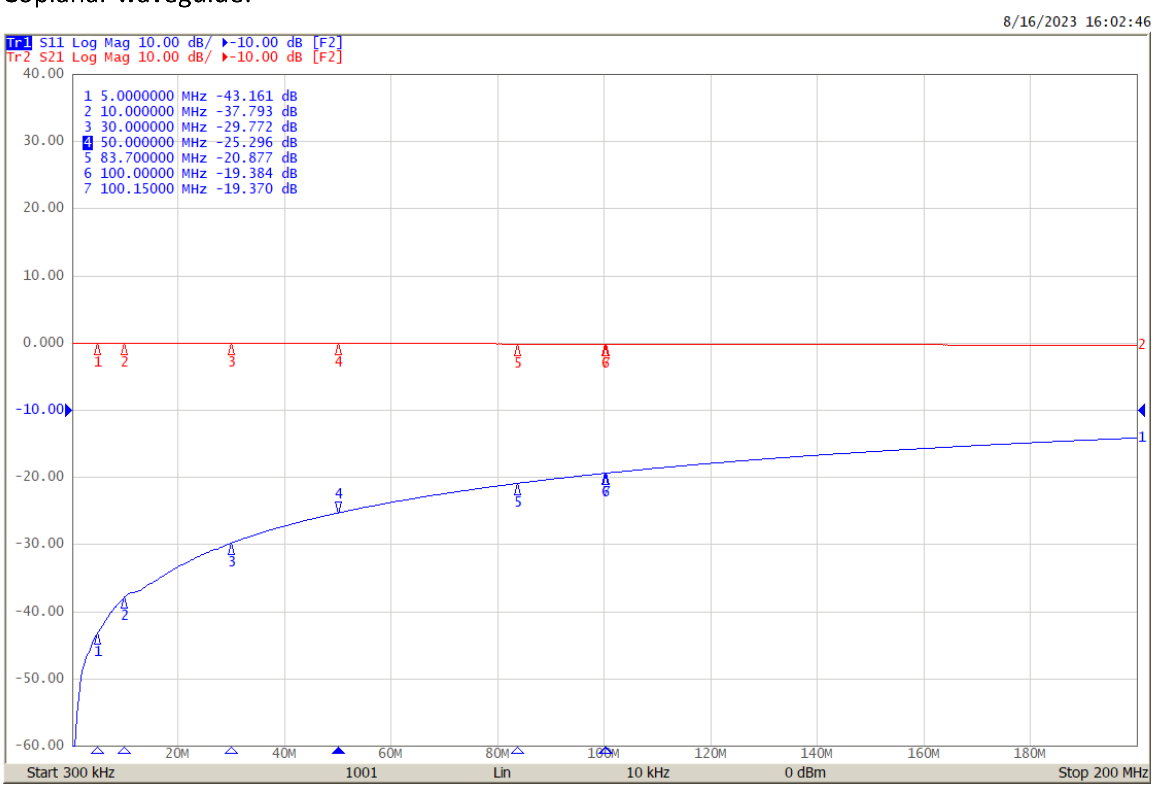
The combined plots are annotated to indicate the filter frequency and Filter Board Numbers used in the measurements. The combined plots share a common scale (10 dB/div) and 0 dB reference (2nd division from top). The traces and marker table along the bottom of each plot are color coded as follows:

- ✓ Plot1 (blue trace): S21 measured on Filter Board 1 (Filter Board 5 for 73.5 MHz LPF)
- ✓ Plot2 (red trace): S11 measured on Filter Board 1 (Filter Board 5 for 73.5 MHz LPF)
- ✓ Plot3 (green trace): S21 measured on Filter Board 2 (Filter Board 6 for 73.5 MHz LPF)
- ✓ Plot4 (magenta trace): S11 measured on Filter Board 2 (Filter Board 6 for 73.5 MHz LPF)
- ✓ Plot5 (black trace): S21 measured on Filter Board 3 (Filter Board 7 for 73.5 MHz LPF)
- ✓ Plot6 (purple trace): S11 measured on Filter Board 3 (Filter Board 7 for 73.5 MHz LPF)

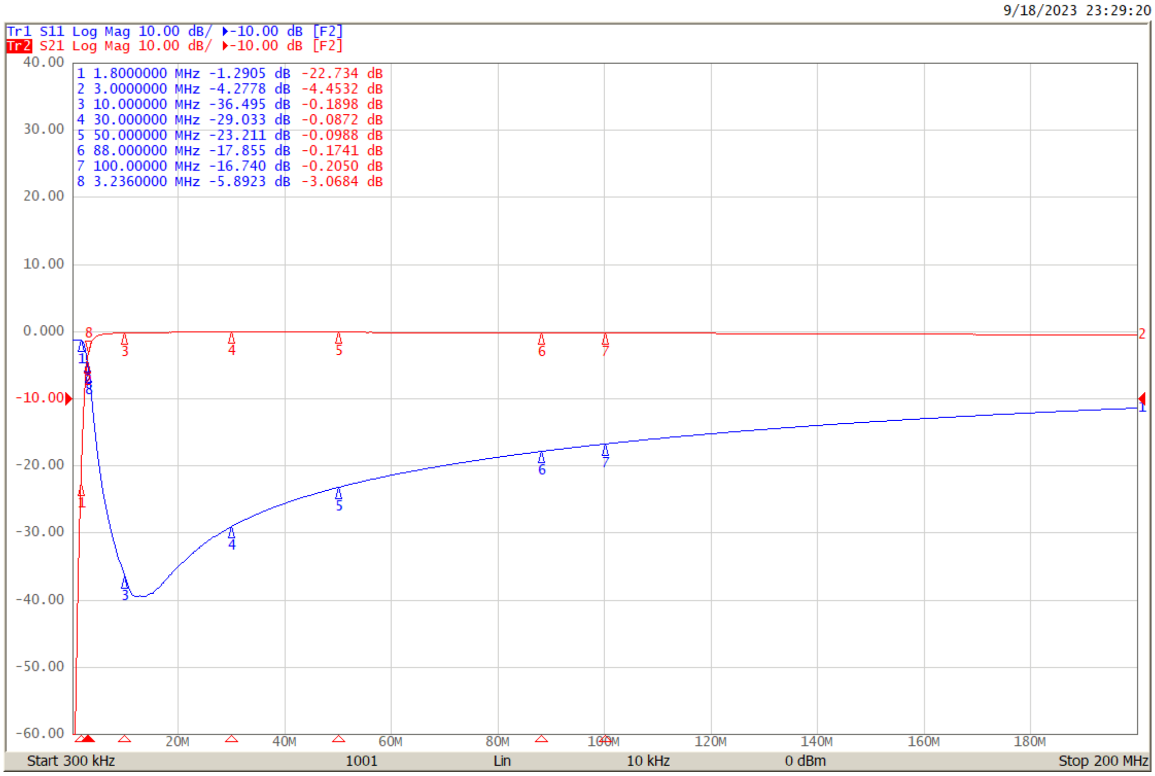
Microstrip:



Coplanar waveguide:

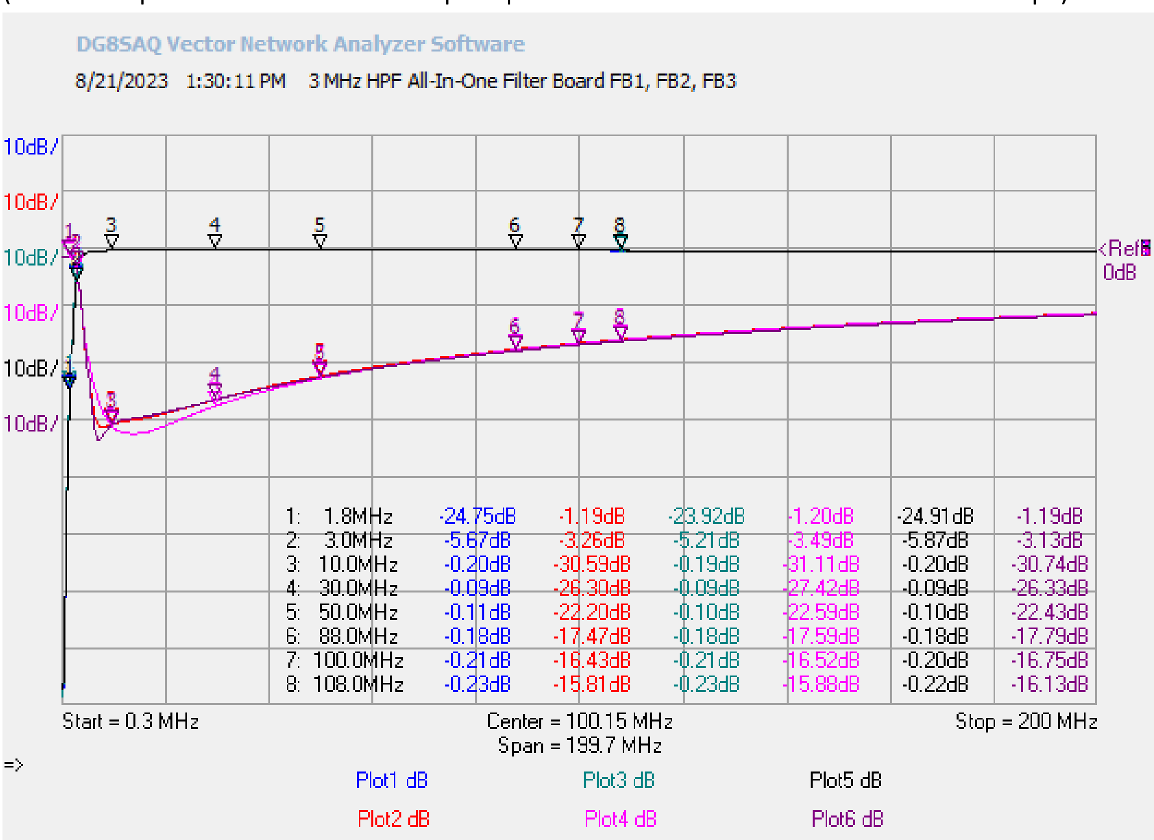


3 MHz Highpass Filter: (Note: this plot is for a filter with 680 pF capacitors, the value used in the final filter)

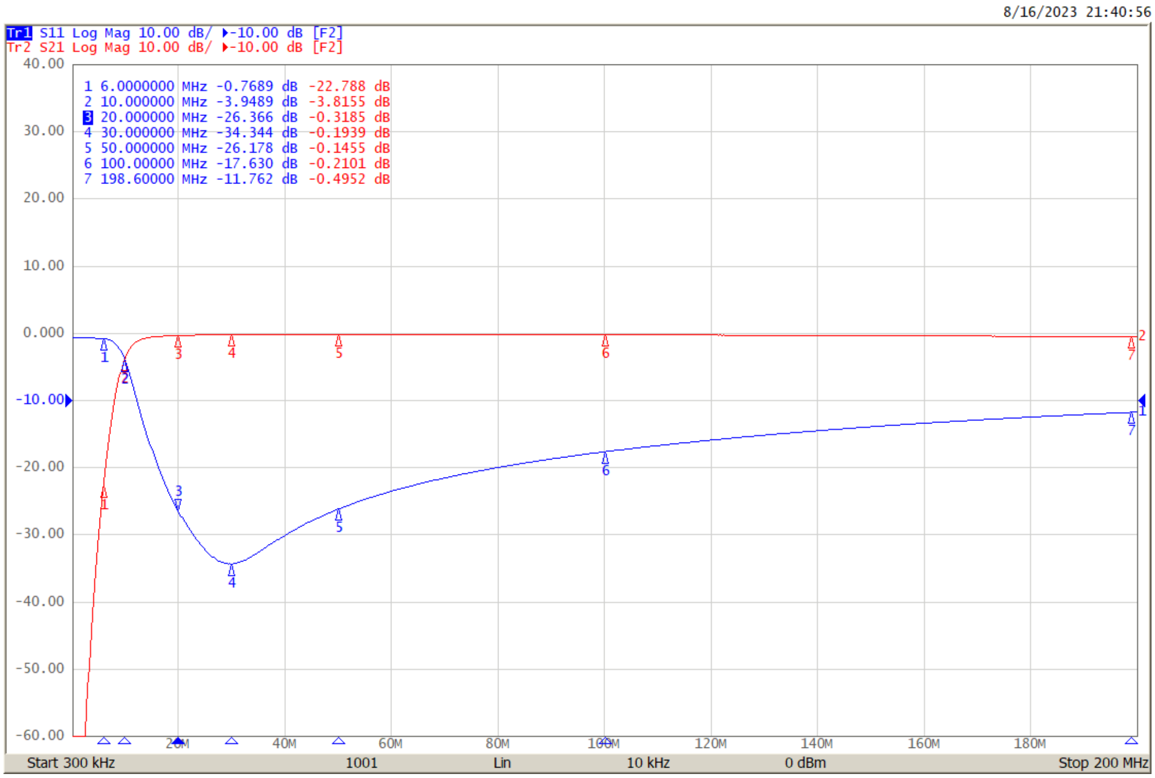


3 MHz Highpass Filter, Combination of three filters:

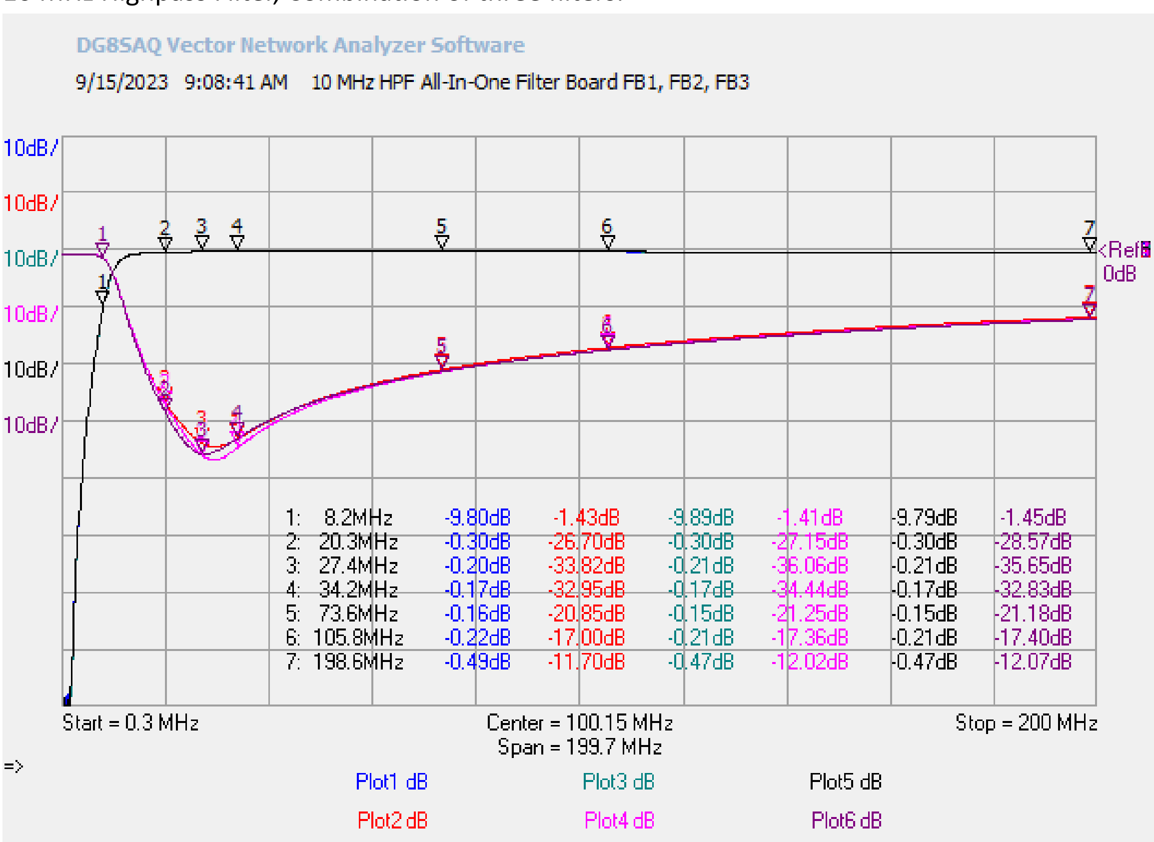
(Note: This plot is for filters with 620 pF capacitors whereas the Rev. I ARX will use 680 pF)



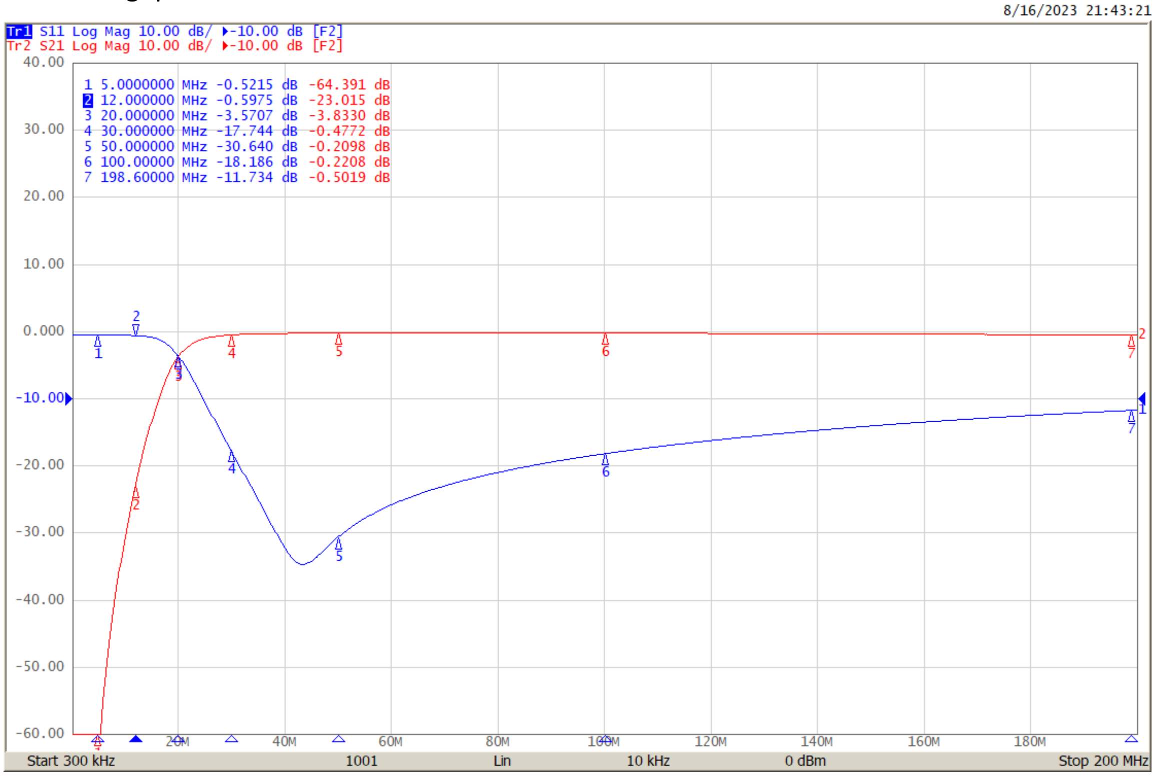
10 MHz Highpass Filter:



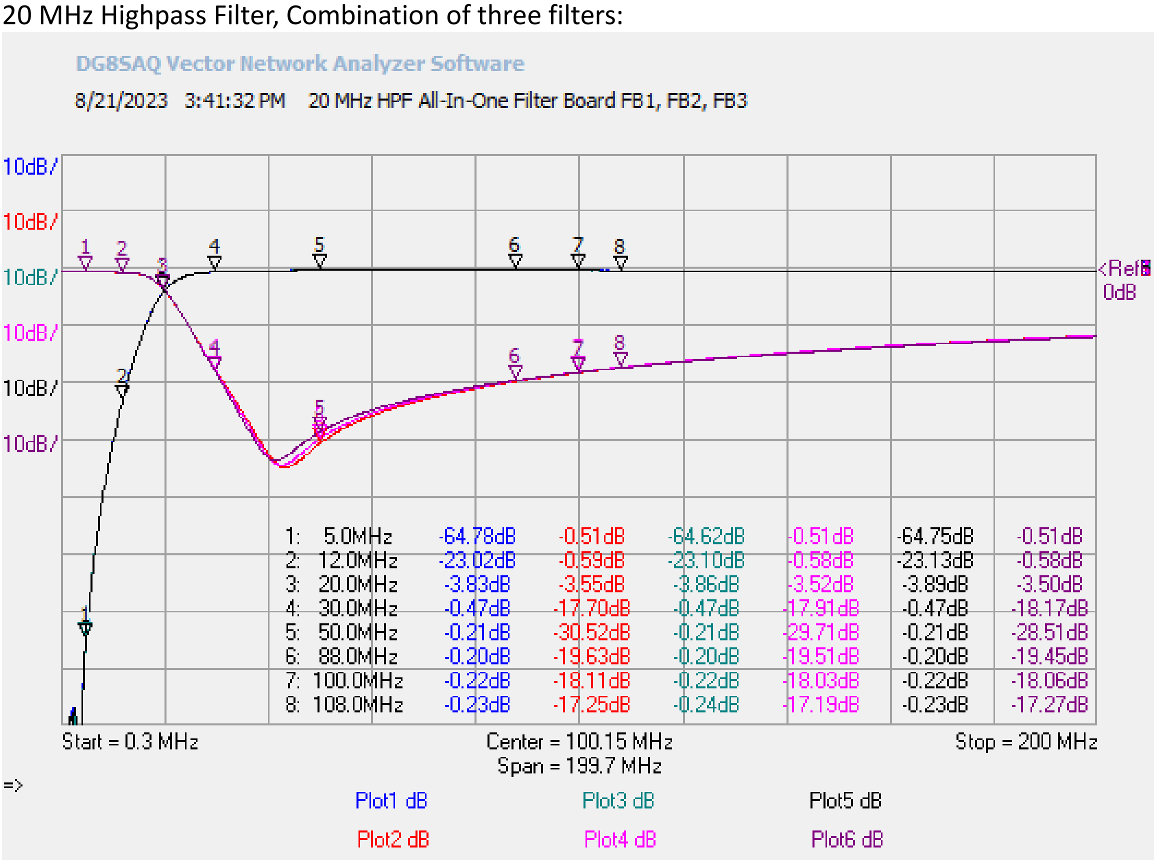
10 MHz Highpass Filter, Combination of three filters:



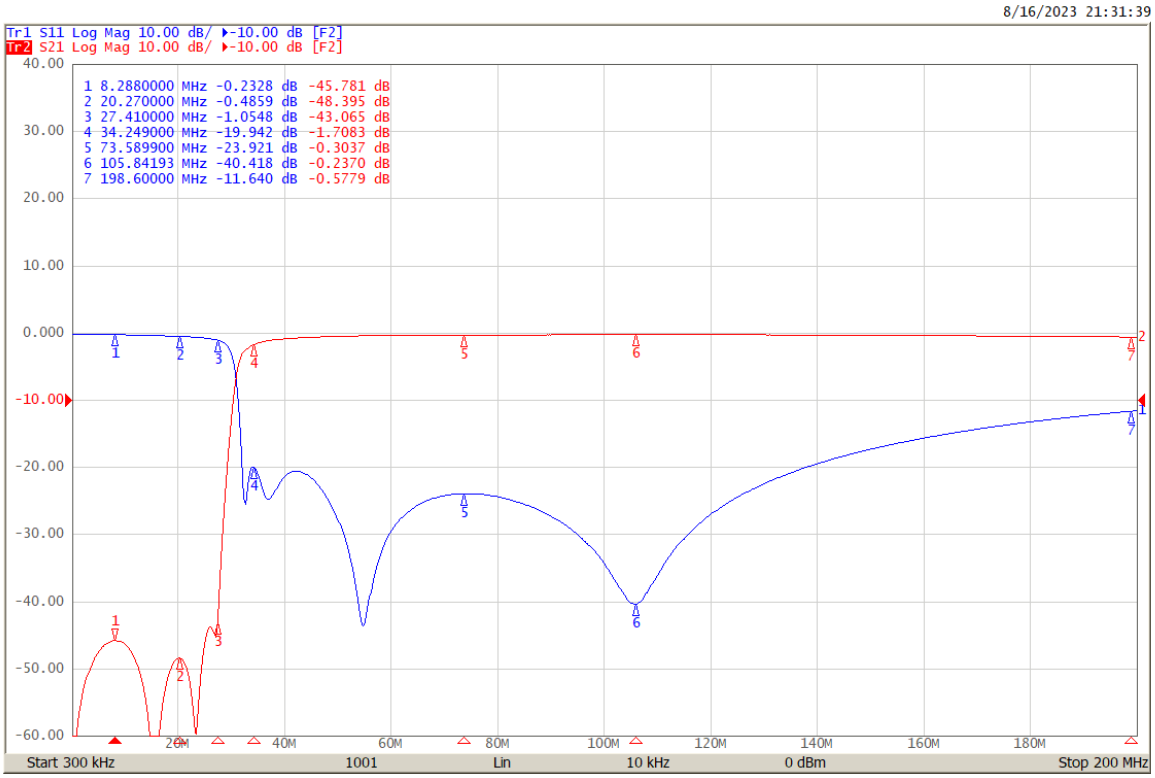
20 MHz Highpass Filter:



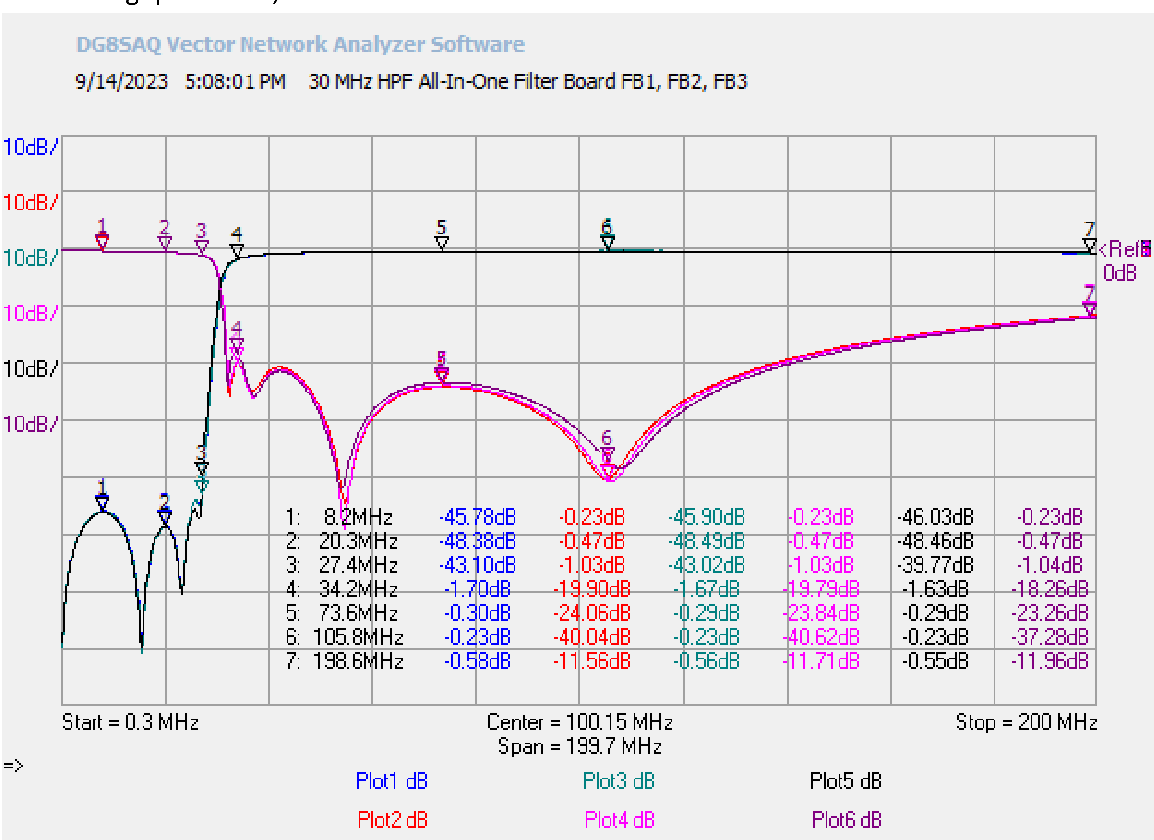
20 MHz Highpass Filter, Combination of three filters:



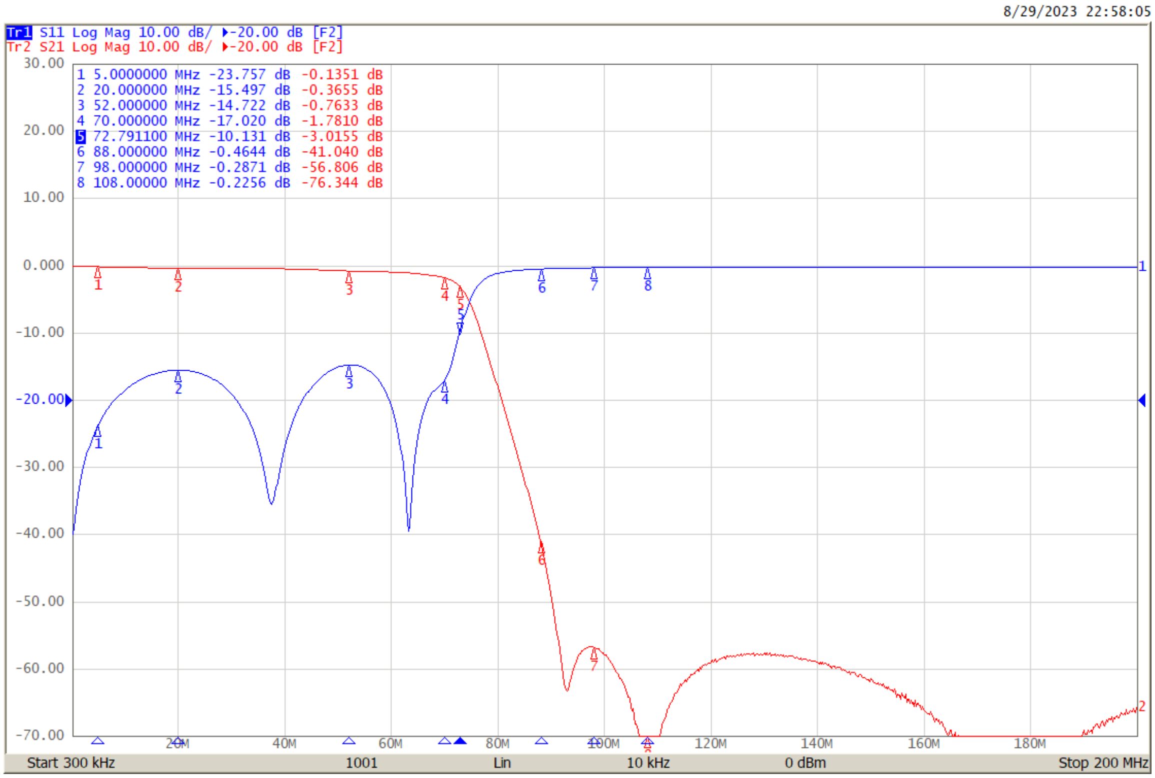
30 MHz Highpass Filter:



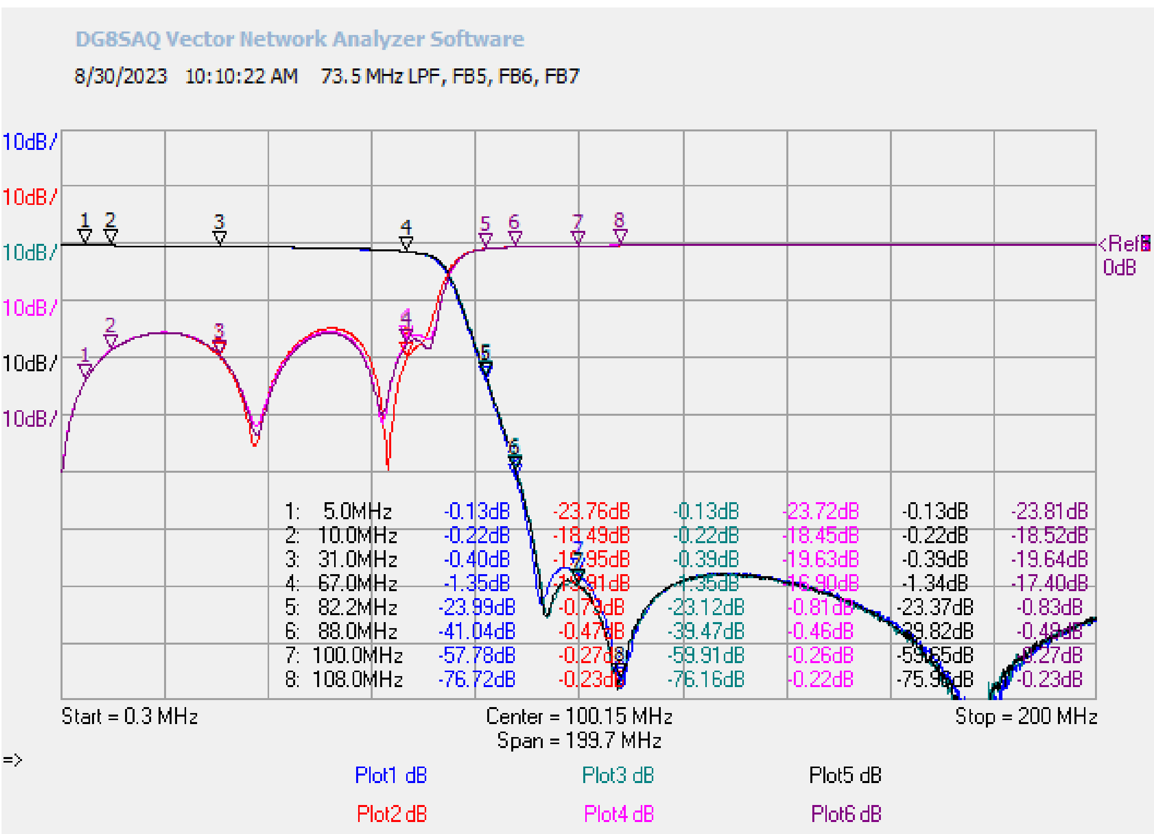
30 MHz Highpass Filter, Combination of three filters:



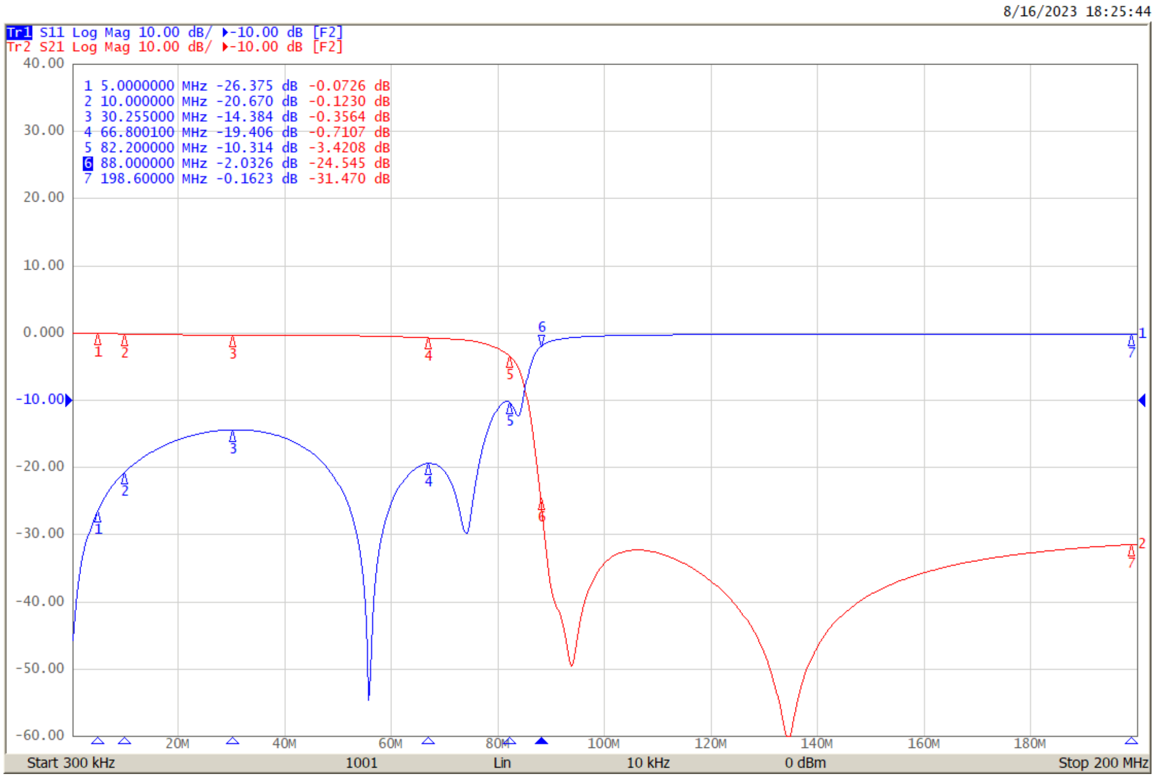
73.5 MHz Lowpass Filter:



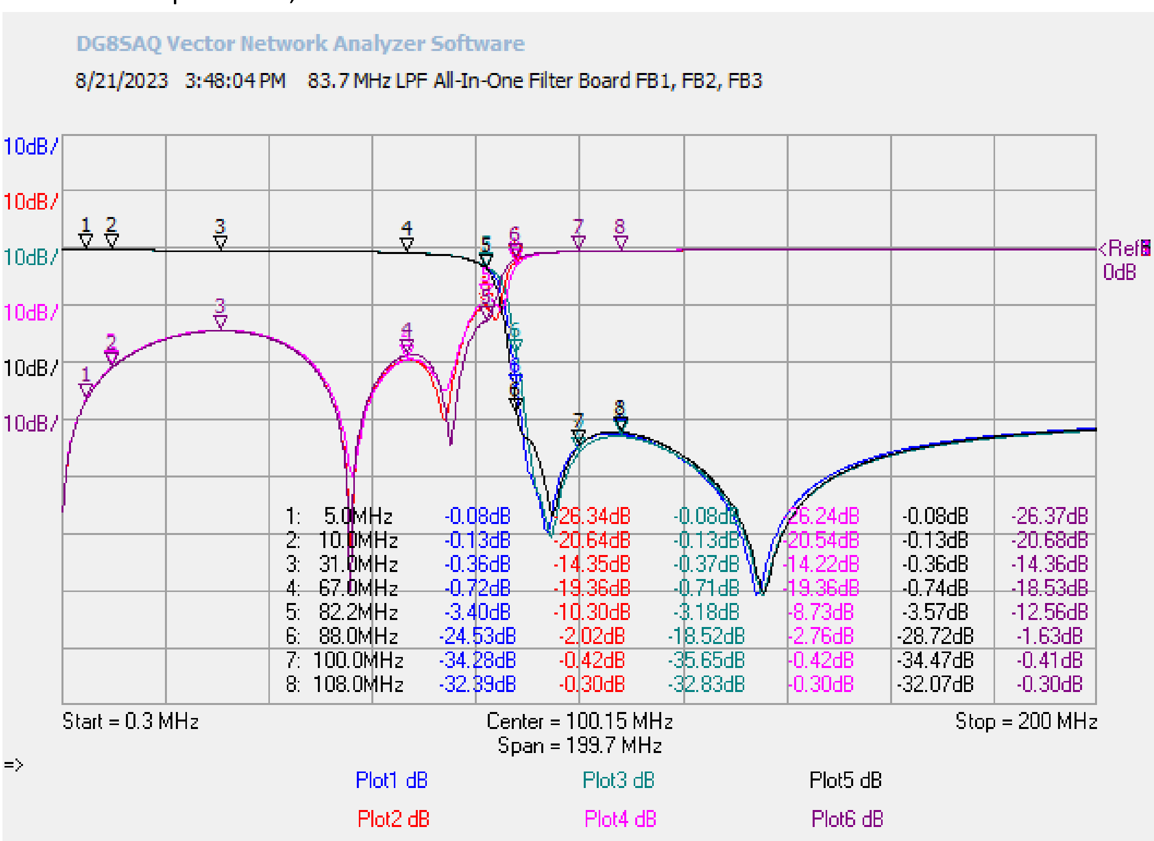
73.5 MHz Lowpass Filter, Combination of three filters:

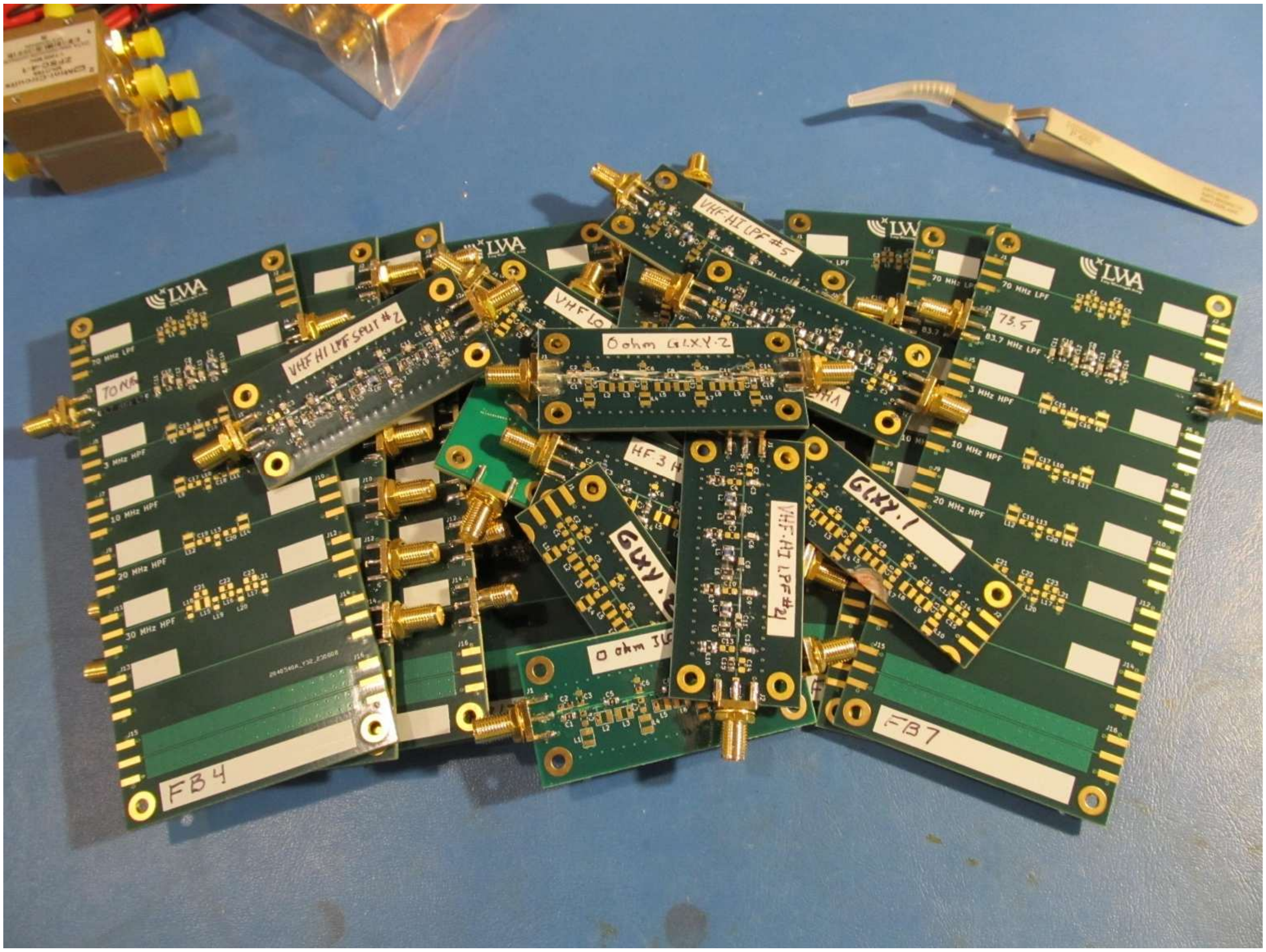


83.7 MHz Lowpass Filter:



83.7 MHz Lowpass Filter, Combination of three filters:



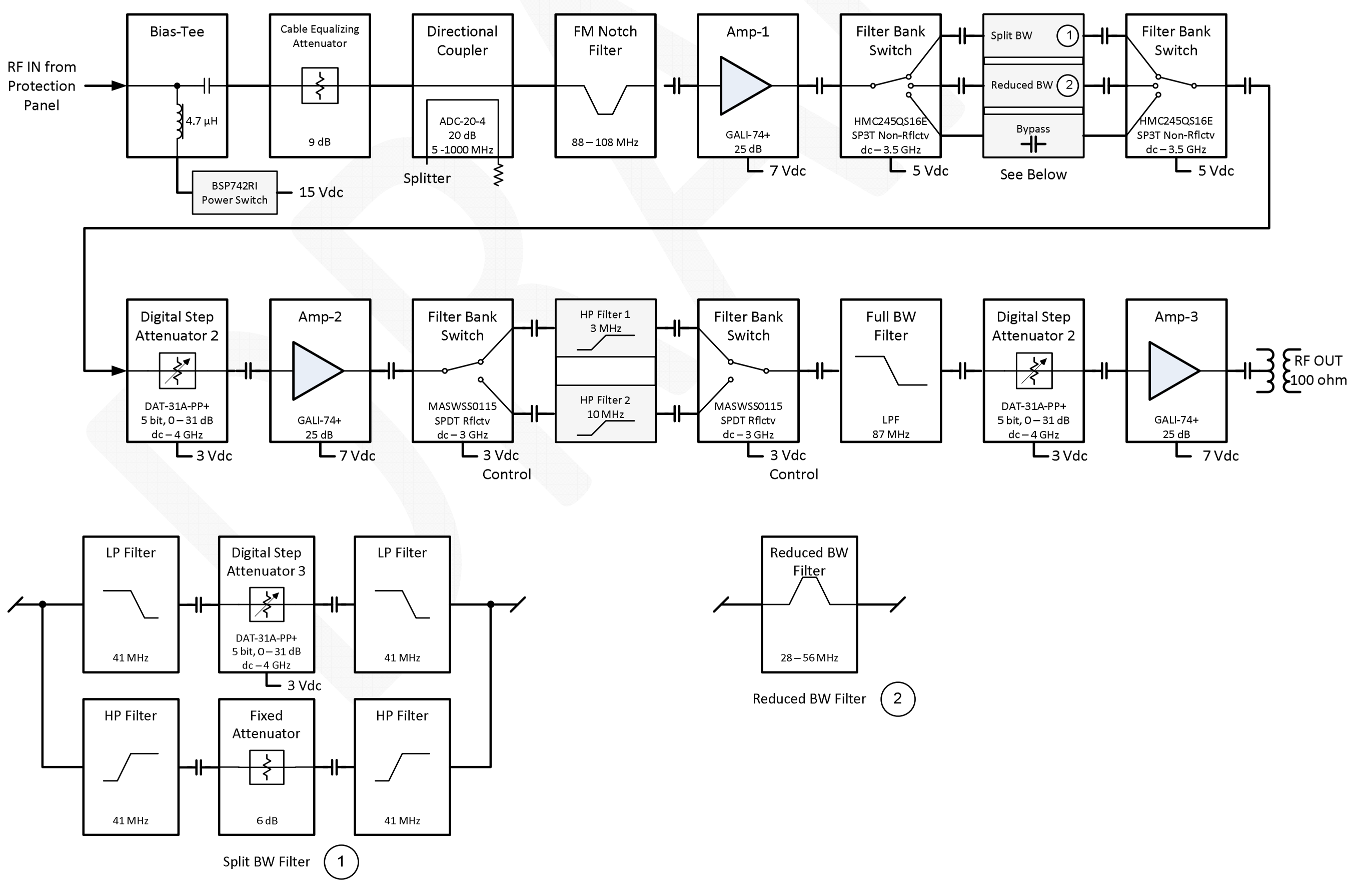

LWA
70 MHz LPF
3 MHz HPF
10 MHz HPF
20 MHz HPF
30 MHz HPF
83.7 MHz LPF
VHF HI LPF SPLIT #2
0 ohm GLXY 2
VHF HI LPF #5
VHF HI LPF #2
GLXY.1
73.5
FB4
FB7

Appendix ~ ARX Rev. G and H Filters

<u>Rev. G ARX filters</u>:

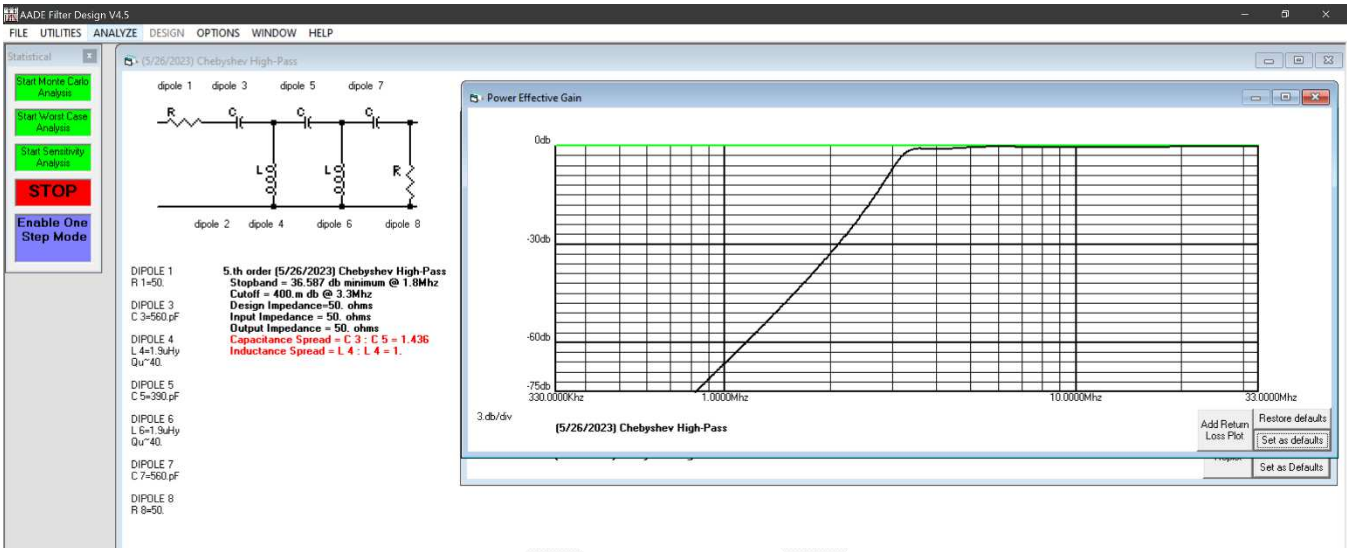
The Rev. G ARX filters and their relationship to the gain and other major blocks in the receiver are shown below. An FM Notch filter is placed immediately before the first gain stage for protection from the FM broadcast band (88 to 108 MHz). This filter was found to introduce ripples in the passband below the notch frequency range. These ripples were then reduced by the 9 dB Cable Equalizing Attenuator in front of the notch filter. Additional details are shown for the two filters in the first filter bank annotated ① and ②. The Split Bandwidth filter in ② is a diplexer that allows varying selection of the attenuation and frequency ranges above and below approximately 41 MHz.

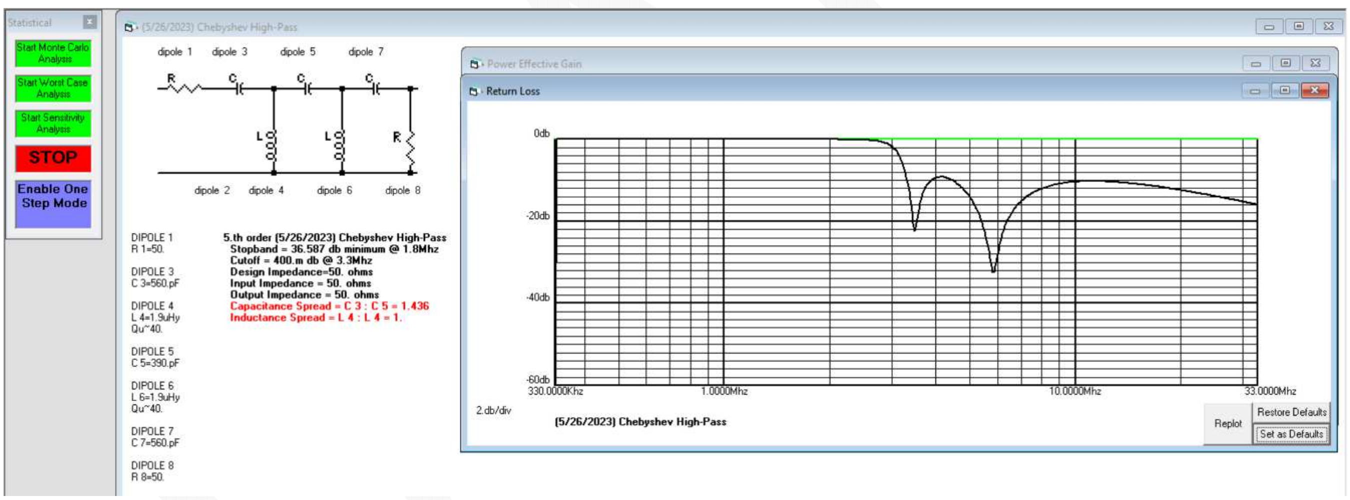
The filter bank immediately following the second gain stage consists of nominal 3 and 10 MHz highpass filters. Simulation shows these have 3 dB cutoff frequencies of 3.2 and 10.5 MHz. The 3 MHz HPF appears to be a Chebyshev type. The 10 MHz HPF is a Butterworth type that uses a T-configuration and has identical response to the proposed Rev. I Butterworth type that uses a Pi configuration. A Full Bandwidth filter is used in front of the last gain stage. This is a lowpass filter with response from dc to just under 88 MHz. Its calculated attenuation at 88 MHz is 3.8 dB.



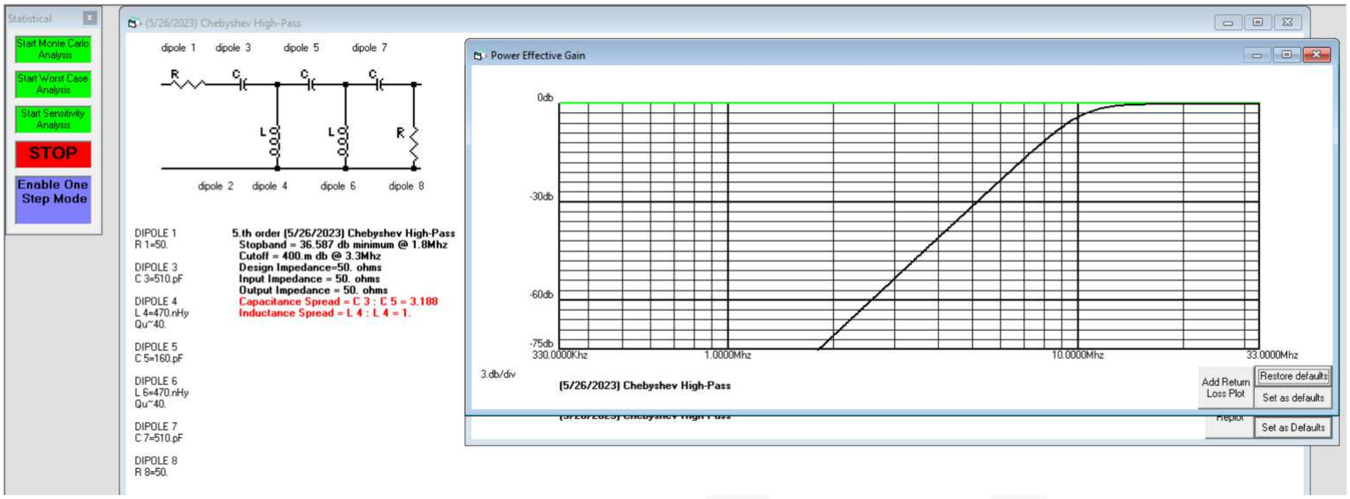
The Rev. G filter schematics are shown below along with plots of the insertion loss and return loss from simulatons. Component values for all filters were taken from the original schematics.

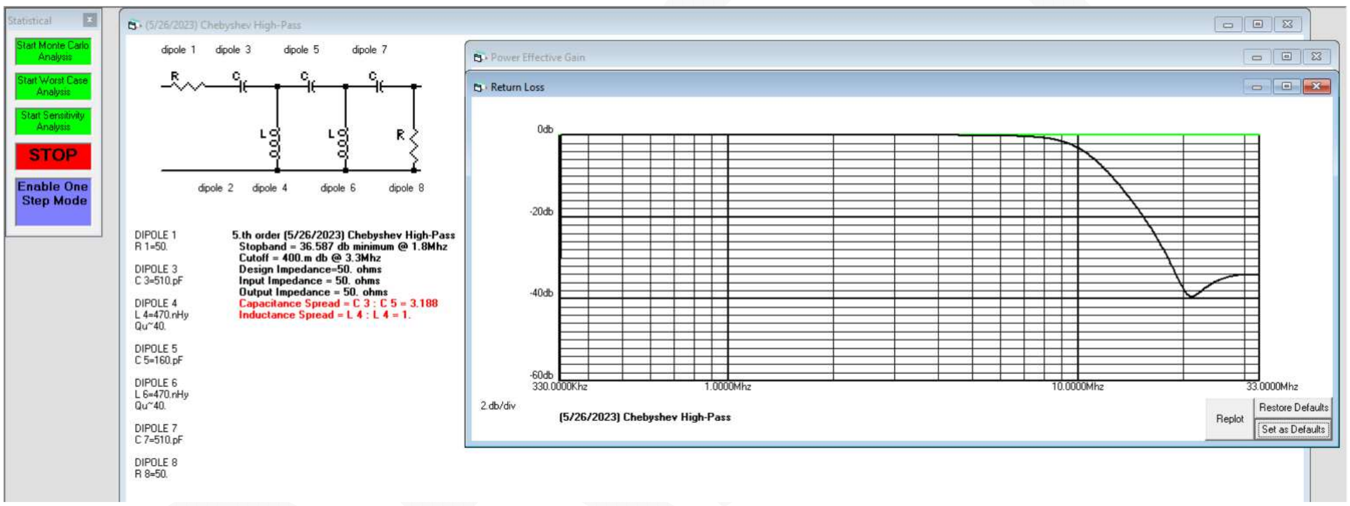
Rev. G 3 MHz Lowpass Filter Insertion Loss and Return Loss:



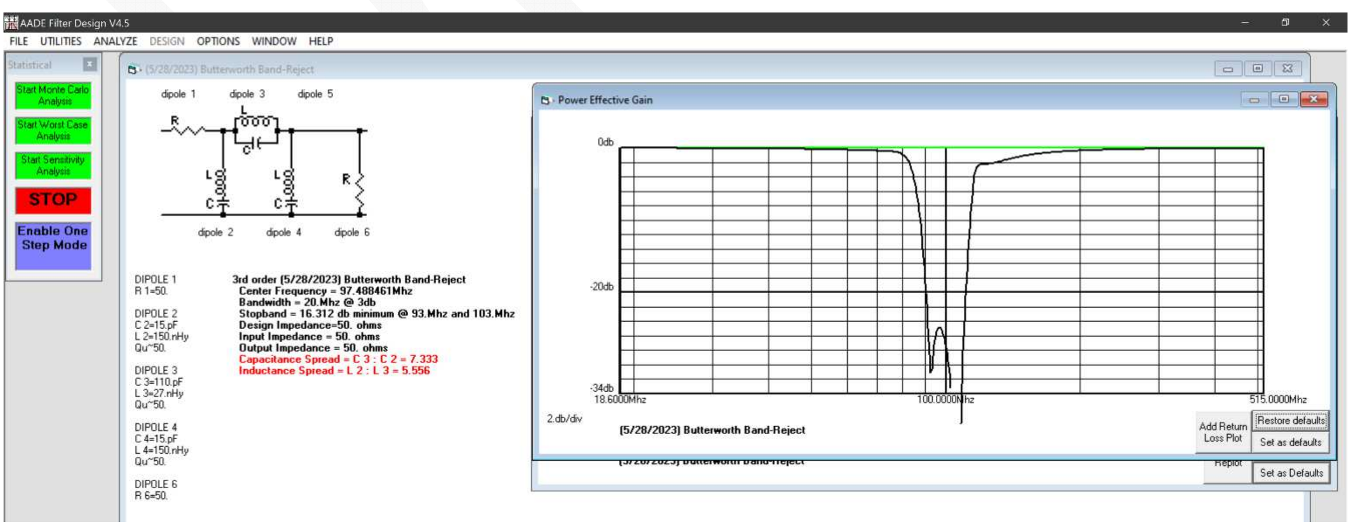


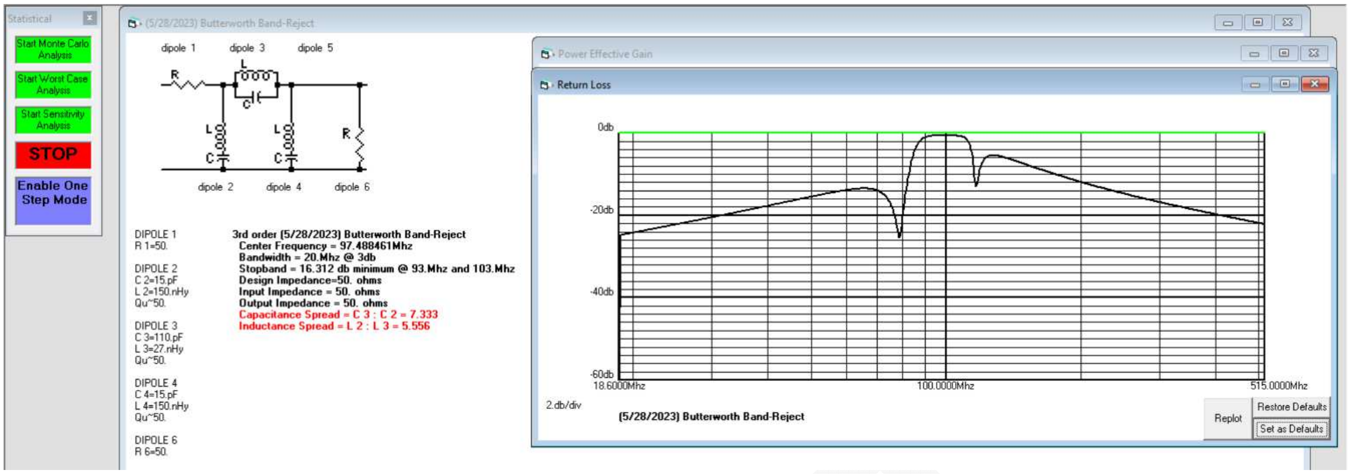
Rev. G 10 MHz Highpass Filter Insertion Loss and Return Loss:





Rev. G FM Broadcast Band Notch filter:

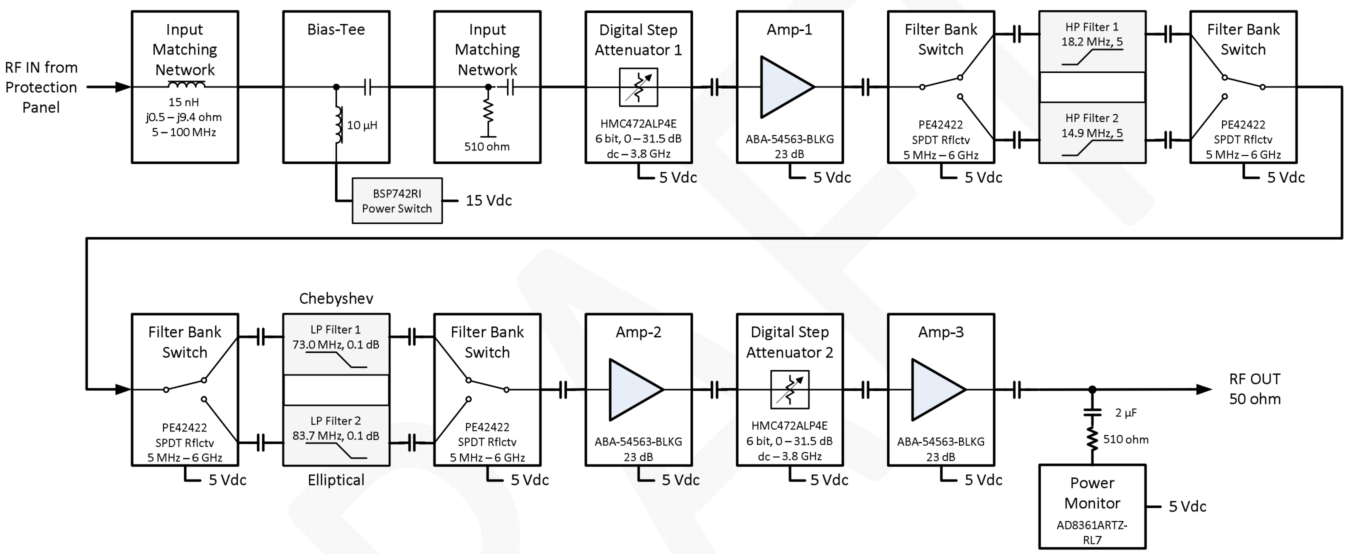



Statistical
Start Monte Carlo Analysis
Start Worst Case Analysis
Start Sensitivity Analysis
STOP
Enable One Step Mode
(5/28/2023) Butterworth Band-Reject
dipole 1
dipole 3
dipole 5
dipole 2
dipole 4
dipole 6
DIPOLE 1
R 1=50.
DIPOLE 2
C 2=15.pF
L 2=150.nHy
Qu~50.
DIPOLE 3
C 3=110.pF
L 3=27.nHy
Qu~50.
DIPOLE 4
C 4=15.pF
L 4=150.nHy
Qu~50.
DIPOLE 6
R 6=50.
3rd order (5/28/2023) Butterworth Band-Reject
Center Frequency = 97.488461Mhz
Bandwidth = 20.Mhz @ 3db
Stopband = 16.312 db minimum @ 93.Mhz and 103.Mhz
Design Impedance=50. ohms
Input Impedance = 50. ohms
Output Impedance = 50. ohms
Capacitance Spread = C 3 : C 2 = 7.333
Inductance Spread = L 2 : L 3 = 5.556
Power Effective Gain
Return Loss
0db
-20db
-40db
-60db
18.6000Mhz
100.0000Mhz
515.0000Mhz
2.db/div
(5/28/2023) Butterworth Band-Reject
Replot
Restore Defaults
Set as Defaults

Rev. H ARX filters:

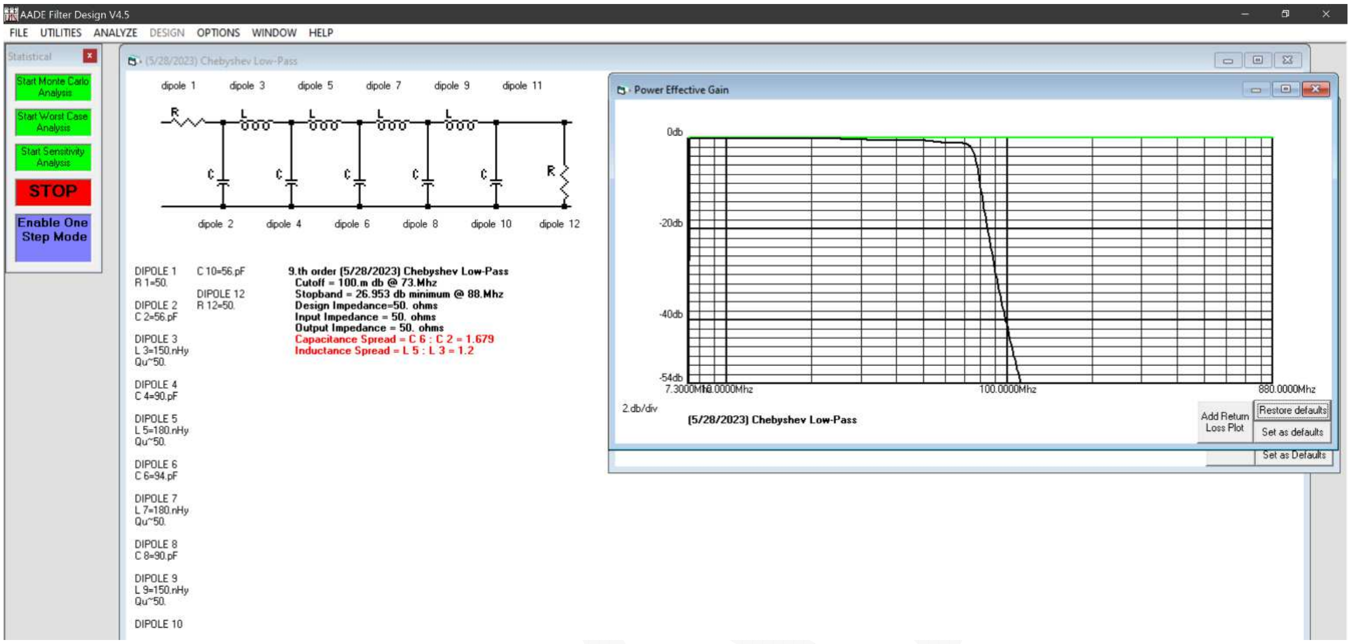
The Rev. H ARX filters and their relationship to the gain and other major blocks in the receiver are shown below. The overall filter scheme in the Rev. H ARX is less complex than the Rev. G ARX. The two highpass filters that follow the first gain stage are 5th order Butterworth designs with design cutoff frequencies of 14.9 and 18.2 MHz.

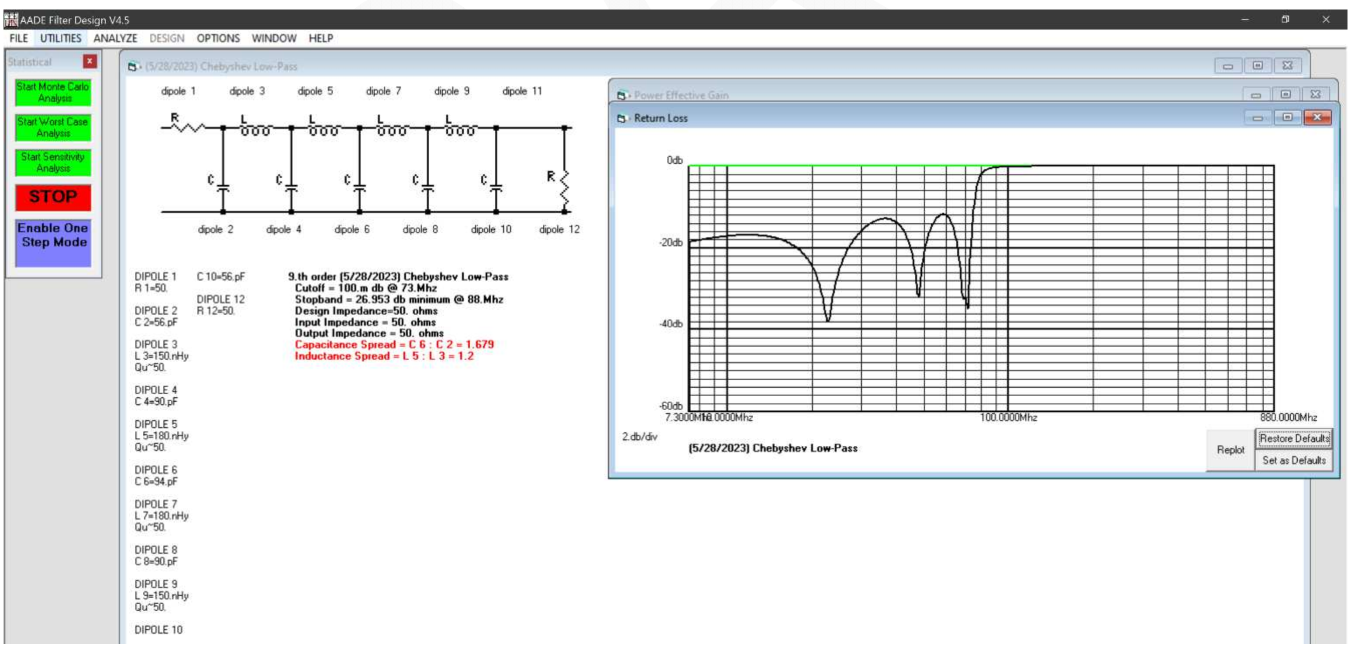
The second filter bank consists of two lowpass filters, a 9th order Chebyshev design with a cutoff frequency of 73.0 MHz and a 7th order Elliptic design with a cutoff frequency of 83.7 MHz. Both filters are designed for 0.1 dB ripple and loss at the cutoff frequency and both are designed to reduce FM broadcast band interference. The 73.0 MHz filter provides 25.7 dB attenuation at 88 MHz, and the 83.7 MHz filter provides 17.5 dB attenuation at 88 MHz.



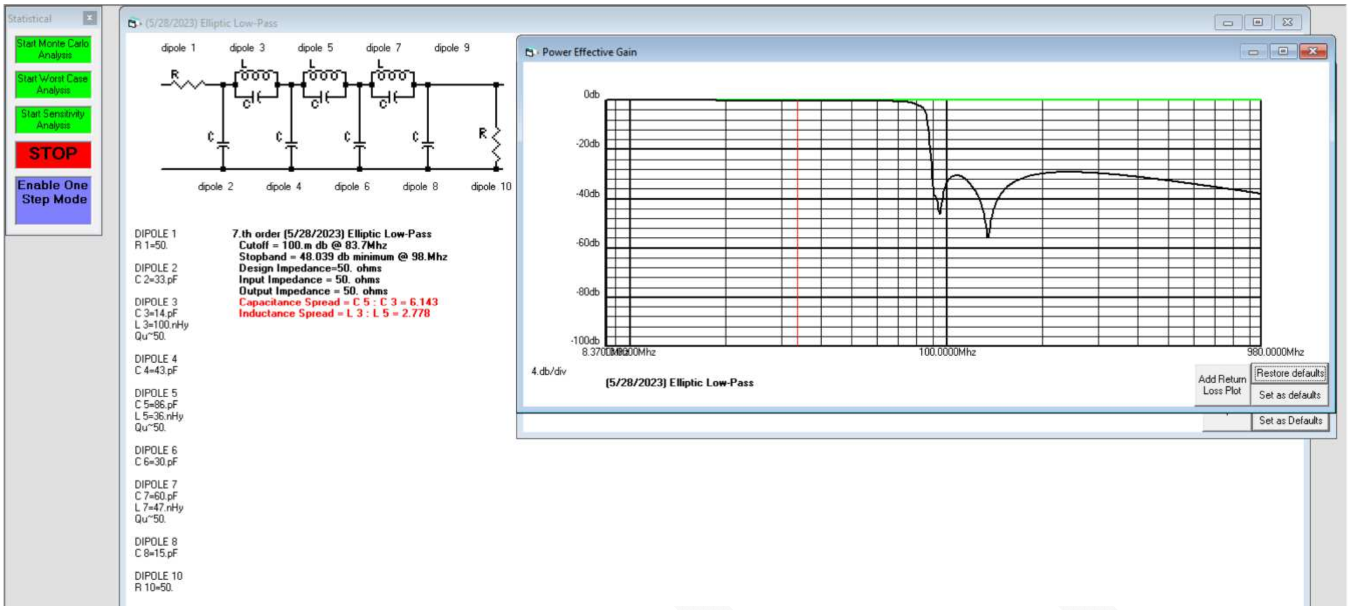
The Rev. H filter schematics are shown below along with plots of the insertion loss and return loss from simulations. Component values for both filters were taken from the original schematics.

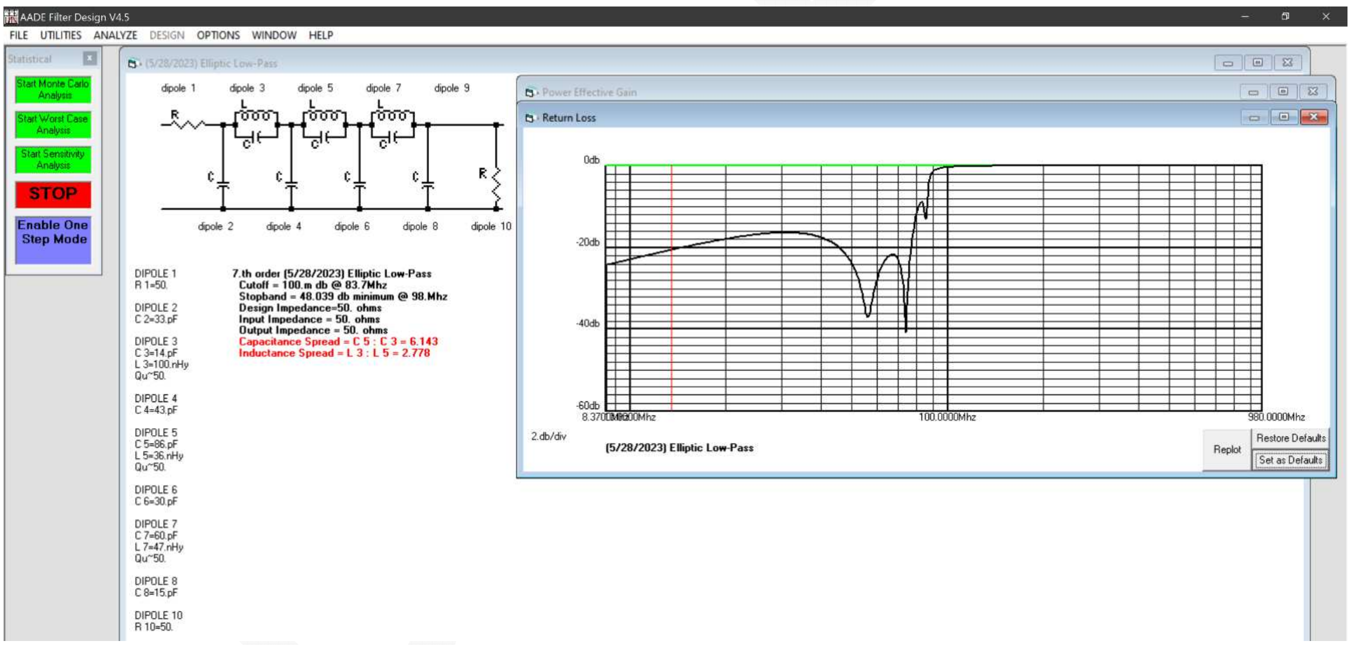
Rev. H 73.0 MHz LPF Insertion Loss and Return Loss:





Rev. H 83.7 MHz LPF Insertion Loss and Return Loss:





Document Information

Author: Whitham D. Reeve

Revisions: 0.0 (Original draft started, 21 May 2023)

0.1 (Edits, 23 May 2023)

0.2 (Transferred Rev. G and H info to his document, 24 May 2023)

0.3 (Added Rev. G and H filter plots, 28 May 2023)

0.4 (Updated 30 MHz HPF, 06 Jun 2023)

0.5 (Revised text and added revised generic filter schematic, 13 Jun 2023)

0.6 (Added Monte Carlo analysis for 83.7 MHz LPF, deleted measurements section, 17 Aug 2023)

0.7 (Added filter PCB design details and filter measurements, 14 Sep 2023)

0.8 (Distribution of draft, 15 Sep 2023)

0.9 (Updated 3 MHz HPF to show 680 pF capacitors, 18 Sep 2023)

1.0 (Removed DRAFT watermark for distribution of final, 20 Sep 2023)

1.1 (Removed system block diagram, 29 Sep 2023)

Word count: 4439

File size (bytes): 13013224

Memo Cover Sheet

ARX-Eval-05

Comparison of ARX Rev. H and Rev. G and I Impedance Matching Networks

30 September 2023

Whitham D. Reeve

Comparison of ARX Rev. H and Rev. G and I Impedance Matching Networks
Whitham D. Reeve

Comparisons: The "Impedance Matching at ARX Coax Inputs" report from CIT for the Rev. H ARX discusses the attempts to optimize the matching of the receiver RF input circuits to the outside plant. It appears there are several important differences between the resulting Rev. H RF input design and the Rev. G and I designs with respect to impedance matching. The designs are compared below as determined from the report and Rev. H ARX schematic. Some aspects of the Rev. H ARX schematic differ from the report, so the information below may not be complete.

1. The Rev. H ARX uses an "isolated" ground for RF circuitry, which is separate from the power and logic ground, whereas the Rev. G and I use a single ground for all circuitry. The "isolated" ground in the Rev. H ARX is tied to the power and logic ground through a 6.8 uH inductor (L18) in parallel with a diode (D4). The characteristics of the inductor and diode and the effects a “split” ground has on the RF input are unknown. Also, the PCB stackup, which defines the layer characteristics of the 4-layer PCB, of the Rev. H ARX is unknown so it is not known if or how ground impedances are controlled. It also is unknown what the physical separation of the two grounds is or how they are configured (except that they are bonded by the inductor/diode as mentioned).

2. The Rev. H bias-tee that couples power to the FEE uses a 10 uH inductor (L1) with 26 MHz self-resonant frequency (SRF) whereas Rev. G uses a 4.7 uH inductor with 90 MHz SRF and Rev. I uses a 10 uH inductor with 165 MHz SRF. The SRF is the frequency where the inductive reactance equals the capacitive reactance of the device. Above the SRF, the device has a capacitive characteristic. In the ARX applications, the bias-tee inductor is a shunt impedance across the RF input. One of the goals of a bias-tee is to make the shunt impedance as high as possible while considering complexity, parts availability and cost. In the Rev. H ARX, the shunt impedance decreases above 26 MHz whereas in the Rev. G and I, the shunt impedance increases with frequency up to 90 MHz (Rev. G) and 165 MHz (Rev. I). A decreasing shunt impedance can complicate impedance matching.

3. The Rev. H ARX RF input has provisions for either coaxial or fiber optic cable feed from the FEE. A 0 ohm resistor (R1 or R2) is used to select one or the other. The Rev. G and I use only a coaxial cable feed. The added circuitry in the Rev. H ARX has an unknown effect on RF performance but the assumption is that the effect is not important.

4. The Rev. H has a transient voltage suppressor (called zener diode D1 in the report) across the input for ESD protection. The initial TVS in the Rev. H ARX had 5 pF maximum shunt capacitance (according to the report) and thus it affected the RF input path impedance matching particularly at higher frequencies. A 5 pF capacitor has 354 ohms reactance at 90 MHz (this would be in parallel with the 50 ohm system impedance). This TVS was replaced with a different part having 0.6 pF *typical* shunt capacitance. The Rev. G uses a transient surge suppressor ON Semi SL15T1G. The Rev. I uses a BAV99LT1G dual switching diode similar to that used in the V2.0 FEE; this device has 1.5 pF maximum capacitance, or 1179 ohms shunt reactance at 90 MHz. The reactance of a capacitor increases with decreasing frequency. An ideal protection device would have 0 capacitance and infinite shunt reactance at all frequencies.

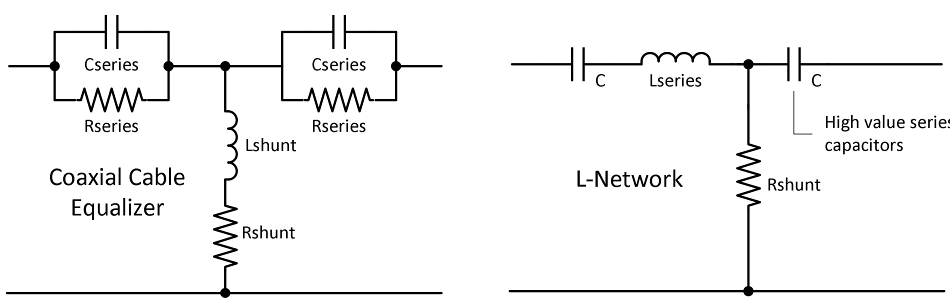
5. The Rev. H ARX has a digital step attenuator after the bias-tee inductor. The attenuator "ACG" (ac ground) pins are connected to the PCB "isolated" ground through capacitors. The initial capacitor values were too small and

later increased to 0.1 µF to improve the low frequency impedance matching. The combined effects of the ACG capacitors and "isolated" ground are unknown.

6. The Rev. H ARX uses an optional impedance matching network that, according to the report, improved overall impedance matching. The network consists of a 15 nH series inductor (2300 MHz SRF and 300 mA maximum rated current) and a 510 ohm shunt resistor. To limit heat dissipation, the resistor is dc isolated from the bias-tee circuits by 0.1 µF series capacitors on each side of its shunt connection. Ideal 0.1 µF dc isolation capacitors have 0.53 ohms series reactance at 3 MHz. Nothing is known about the characteristics of these capacitors at VHF or about the inductance change of the series inductor when the FEE operating current (about 250 mA) is 83% of the inductor's rated current (300 mA).

ARX Rev. I RF Input: The Rev. I RF input will have optional circuitry, in the form of PCB SMD pads, for an impedance matching network but its exact form needs to be determined by additional work. The CIT report cited above has some outside plant measurements that may be useful. The return loss of the FEE output is quite good (> 20 dB from about 10 to 90 MHz), indicating a good match to the 50 ohm system impedance, so it probably can be assumed that the outside plant and cable entrance panel are the main source of impedance variations.

Impedance matching possibilities are a coaxial cable equalizer network or a simple L-network, the latter is similar to the Rev. H. design (see basic schematics below). It may be possible to layout the PCB to accommodate either network and the SMD pads can be populated as required, but any unused SMD pads will add capacitance to the RF path, which is known to be detrimental to impedance matching at VHF. Any network on the input will be a compromise because of the widely varying cable lengths involved in the LWA.



The cable equalizer is not actually an impedance matching network but is designed to provide decreasing loss with increasing frequency, opposite of a coaxial cable. An L-network made from a series inductor and shunt resistor, as in the Rev. H design, compensates for capacitive reactance in the outside plant and reduces the real part of the impedance (according to the report).

The L-network is the preferred impedance matching method. It is shown in the above schematic with the inductor inside the isolation of high-value coupling capacitors to eliminate inductance changes with FEE load current.

Document Information

Author: Whitham D. Reeve

Revisions: 0.0 (Original draft started, 15 Jun 2023)
0.1 (Updated 19 Jun 2023)
0.2 (Updated for distribution, 30 Sep 2023)

Word count: 1135
File size (bytes): 43520

Memo Cover Sheet

ARX-Eval-06

GALI-74+ Amplifier Performance Measurements

3 October 2023

Whitham D. Reeve

GALI-74+ Amplifier Performance Measurements

Whitham D. Reeve

This document discusses measurements of the Mini-Circuits (MCL) GALI-74+ amplifier at various supply voltages and may be used as an aid in deciding to use the existing LWA power supplies or replace them. All measurements described here use the MCL TB-409-74+ Evaluation Board with the GALI-74+ amplifier. All measurements were made at room temperature (20 °C), and no attempt was made to determine the device characteristics at other temperatures.

The GALI-74+ amplifiers in the Rev. G ARX use a 7 Vdc supply voltage derived from the 8 Vdc bus. 7 Vdc is the minimum supply voltage (Vcc) listed in the device datasheet. The same amplifiers are used in the Rev. I ARX, and it was thought that increasing the supply voltage may improve device (and receiver) performance. The measurements discussed below indicate that, at least under the conditions tested, there are no practical differences across the MCL recommended voltage range.

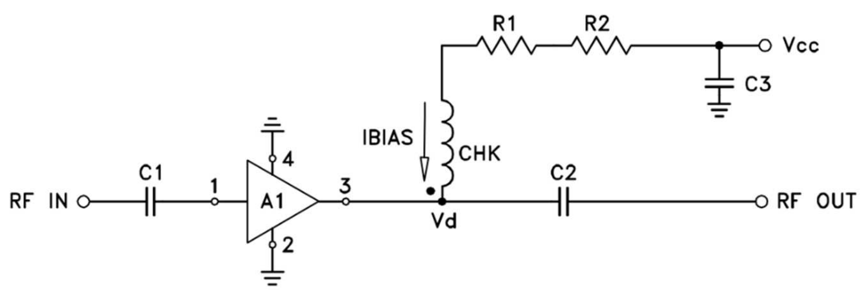
The existing 8 Vdc bus power supplies can be adjusted for 8.8 Vdc operation without replacing the power supplies or associated systems. Voltages higher than 8.8 Vdc require costly power supply replacements and other changes, all of which are not yet known.

It is noted that the 7 Vdc bus voltage regulator (LM1084) on each PCB in the Rev. G ARX has no margin in its dropout voltage. Specifically, the dropout voltage given in figure 1 of the LM1084 datasheet shows a dropout of 1.0 V at the estimated load of 2 A (the entire PCB) at 25 °C. This is a typical value that varies with temperature and device manufacturing; there is no specified maximum dropout voltage given in the datasheet. It may be possible to find a voltage regulator for the Rev. I ARX that has a lower dropout voltage. In any case, it is recommended that the new PCBs be operated with the 8 V power supplies adjusted to 8.8 Vdc to ensure adequate dropout margin.

The measurements discussed here are:

- S-parameter measurements including S11, S21, S12 and S22, 5 to 200 MHz
- Noise figure measurements (10 to 200 MHz)
- 1 dB compression measurements (40 MHz)

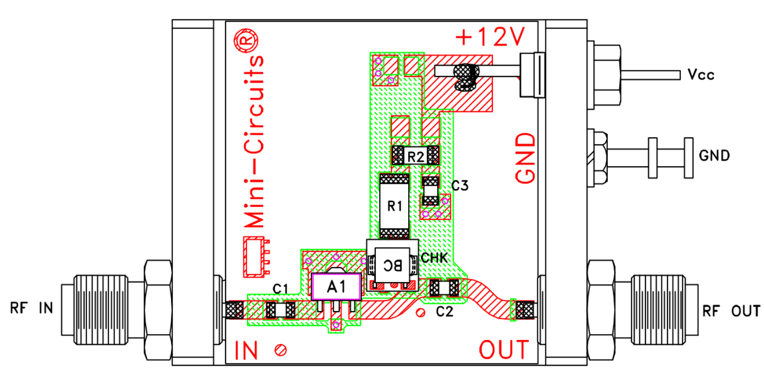
<u>Evaluation Board modifications</u>: The measurements require modification of the TB-409-74+ Evaluation Board for lower frequencies and different supply voltages. The RF choke CHK, MCL p/n TCCH-80+, is replaced with a Coilcraft p/n 1008CS-472 (4.7 µH) inductor, and the 2400 pF input and output coupling capacitors C1 and C2 are replaced with 0.1 µF MLCC. The board is further modified for each set of supply voltage measurements by replacing the R1 and R2 bias resistors as shown in the schematic and table below.



Vcc	Bias resistor R1 (ohms)	Bias resistor R2 (ohms)	Bias resistor R1+R2 (ohms)	Datasheet (ohms)	Remarks
7	27.4	1.2	28.6	28.7	
7.5	33.0	2.0	35.0	N/A	Estimated bias resistors
8	41.2	0	41.2	41.2	
9	53.6	0	53.6	53.6	
10	66.5	0	66.5	66.5	
11	78.7	0	78.7	78.7	
12	68.1	22.6	90.7	90.9	

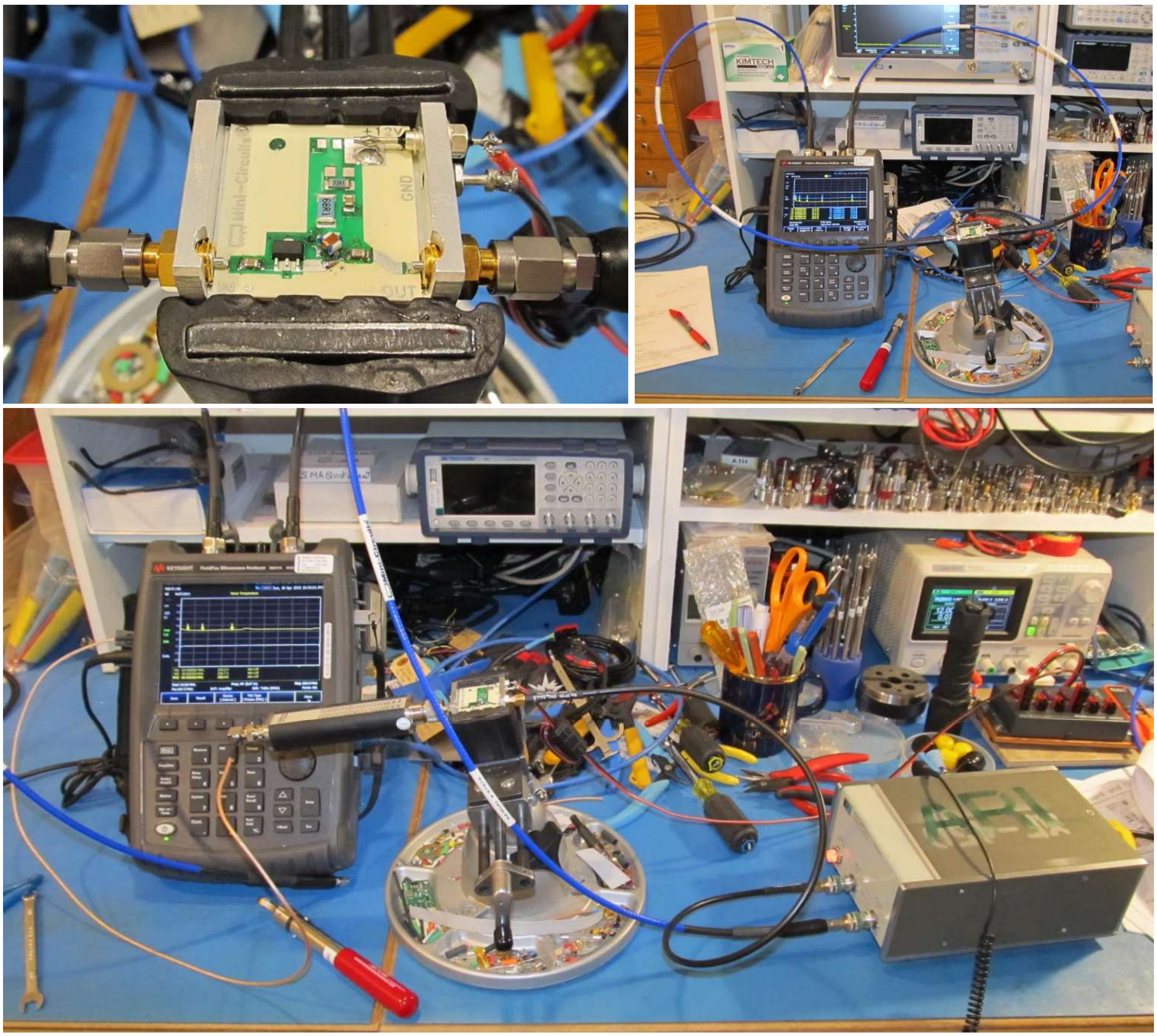
The above resistor values are from the GALI-74+ datasheet (except 7.5 V) and do not take into account the resistance of the bias-tee inductor. The original bias-tee inductor (RF choke) on the evaluation board has a typical dc resistance of 0.1 ohms, which is relatively small compared to the specified total bias resistance. However, the replacement inductor has a dc resistance up to 4 ohms. This increased resistance inadvertently was not taken into account when purchasing the resistors for the evaluation. Since this resistance is significant at the lower supply voltages, the supply voltage Vcc at each increment was increased slightly to provide a device bias current of 78 mA. See table below, which includes the measured device voltage at each supply voltage. According to the datasheet the optimum bias current is 80 mA but actually was set slightly lower.

Vcc (V)	Actual Vcc (V)	Bias current (mA)	Device voltage Vd (V)	Remarks
7	7.00	70	4.7550	Initial setting, no measurements
7	7.30	78	4.7820	Final setting
7.5	7.80	78	4.7793	Vcc not listed in datasheet
8	8.25	78	4.7738	
9	9.20	78	4.7766	
10	10.23	78	4.7852	
11	11.10	78	4.7656	
12	12.00	77	4.7677	



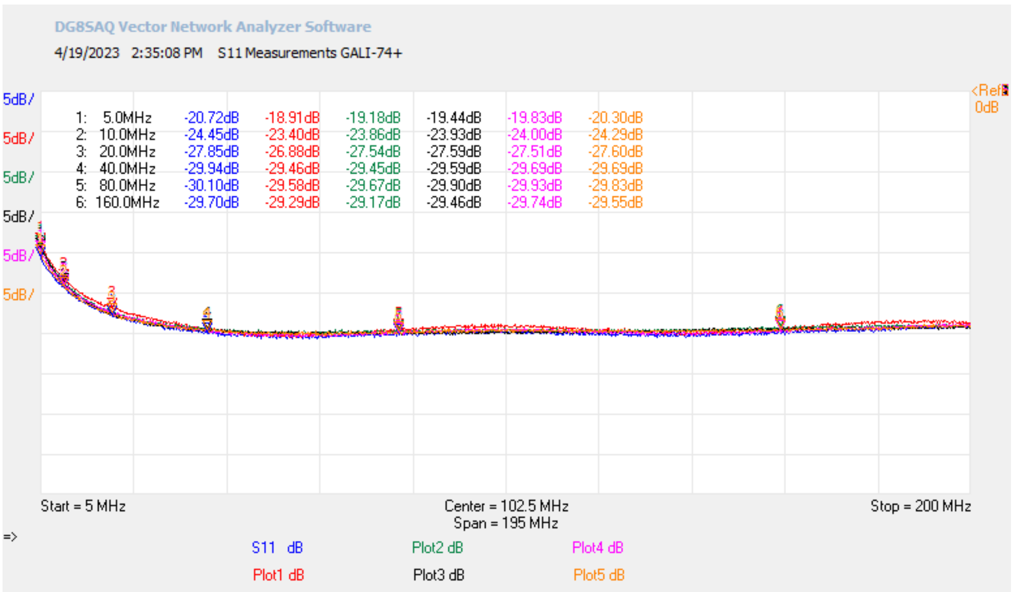
Mini-Circuits TB-409-74+ Evaluation Board. Bias resistor R1 is size 2010 rated 3/4 W and R2 is size 0805 rated 1/10 W. The RF choke CHK is not a standard size and was replaced with a 4.7 µH Coilcraft part (p/n 1008CS-472XGRC, 2%) installed at an angle to reach to two pads. Also, C1 and C2 were replaced with 0.1 µF 0805 parts to improve the evaluation board low frequency response. See Appendix for before and after images of the evaluation board.

Test equipment: The S-parameters were measured with a FieldFox N9917A in Network Analyzer mode and calibrated with a Mini-Circuits KSOLT-63+ calibration kit. The noise figure was measured with the N9917A in Noise Figure mode and an HP 346A noise source with 6 dB excess noise ratio (ENR). An HP 8447A amplifier was used with the N9917A to lower N9917A receiver noise figure for the measurements; the N9917A is calibrated for noise figure measurements with the external amplifier. A Rohde & Schwarz SMC100A RF signal generator and Siglent SSA 3032X spectrum analyzer were used for the 1 dB compression measurements. The 1 dB compression point is a difference measurement, so calibration is not critical. The evaluation board was powered by a Siglent SPC3303X 3-channel variable output power supply. All test cables were MCL CBL-1M-SMNM+.



Test setups: Upper-left: Modified evaluation board. The replacement bias-tee inductor near the lower-middle had to be mounted at an angle to reach the two pads. Upper-right: S-parameter measurements; Lower: Noise figure measurements. The evaluation board is mounted in a bench vise near the middle-left, and it is connected to the noise source. The noise source is powered by the N9917A internal Voltage Variable Source (VVS). The external amplifier is seen in the lower-right of the image and the power supply for the evaluation board is seen near the upper-right.

S-parameters: Although all four S-parameters were measured and recorded, only S11 (equivalent to input return loss) and S21 (equivalent to forward gain) are shown in the plots below. There are no discernible differences in either parameter across the voltage range 7.3 to 11.1 V. The traces for Vcc = 12.0 V are not shown due to limitation in the software used to plot the data but they are identical to the others.



GALI-74+ S11 Key:

Plot1 (red) 7.3 V;

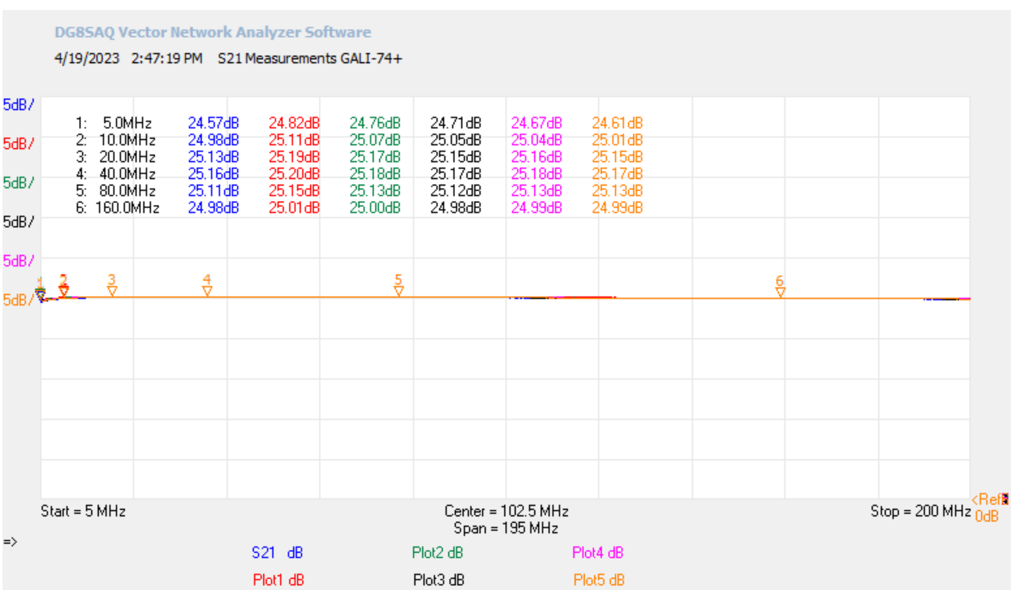
Plot2 (green) 7.8 V;

Plot3 (black) 8.25 V;

Plot4 (magenta) 9.20 V;

Plot5 (orange) 10.23 V;

S11 (blue) 11.10 V



GALI-74+ S21 Key:

Plot1 (red) 7.3 V;

Plot2 (green) 7.8 V;

Plot3 (black) 8.25 V;

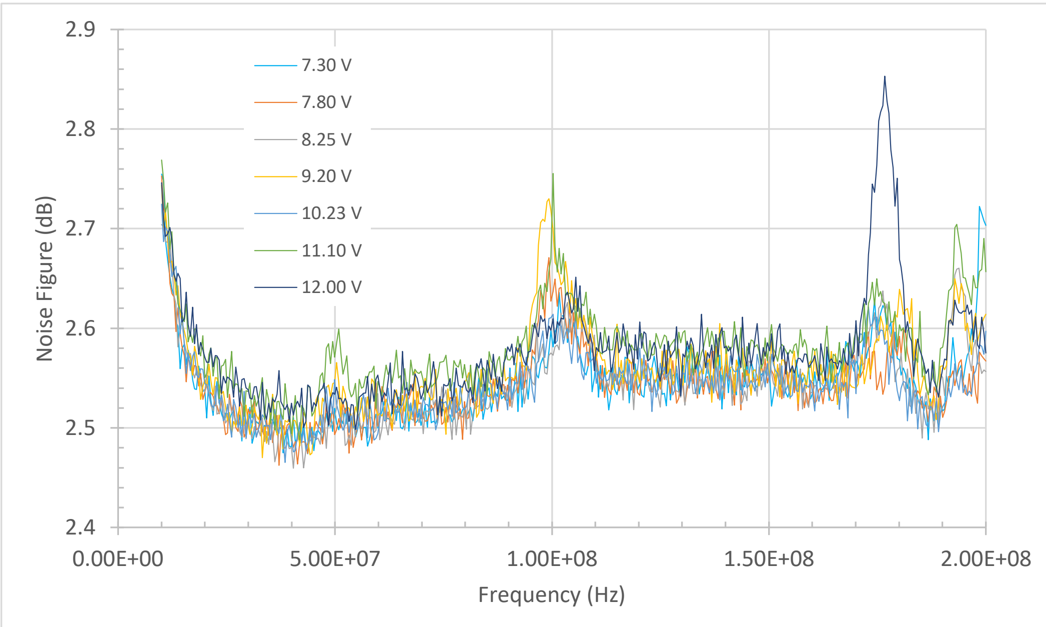
Plot4 (magenta) 9.20 V;

Plot5 (orange) 10.23 V;

S11 (blue) 11.10 V

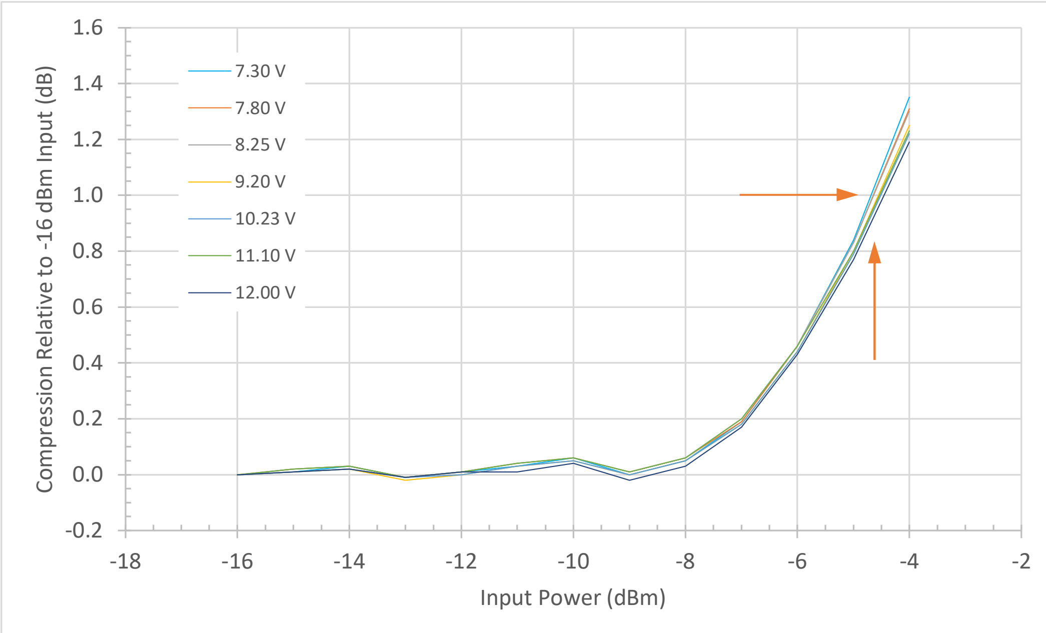
Noise figure: The GALI-74+ noise figure was measured with a calibrated 6 dB ENR noise source and the Fieldfox instrument in Noise Figure mode. In addition to the FieldFox, an external low noise amplifier was used in the measurements to lower the system noise figure. The external amplifier was calibrated as part of the system for these measurements. Because the FieldFox is limited to a low frequency of 10 MHz when in the Noise Figure mode, the frequency range of the measurements covered 10 to 200 MHz.

The plots appear to show a slightly higher noise figure at the higher voltages whereas the noise figure plots at the lower voltages overlay very closely. However, the variations fall within the inherent uncertainty with these types of measurements. The peak near 100 MHz likely is from FM broadcast station interference and the peak near 175 MHz likely is from TV broadcast station interference. Both peaks varied slightly with each sweep of the instrument and are exaggerated in the plots because of the scale.



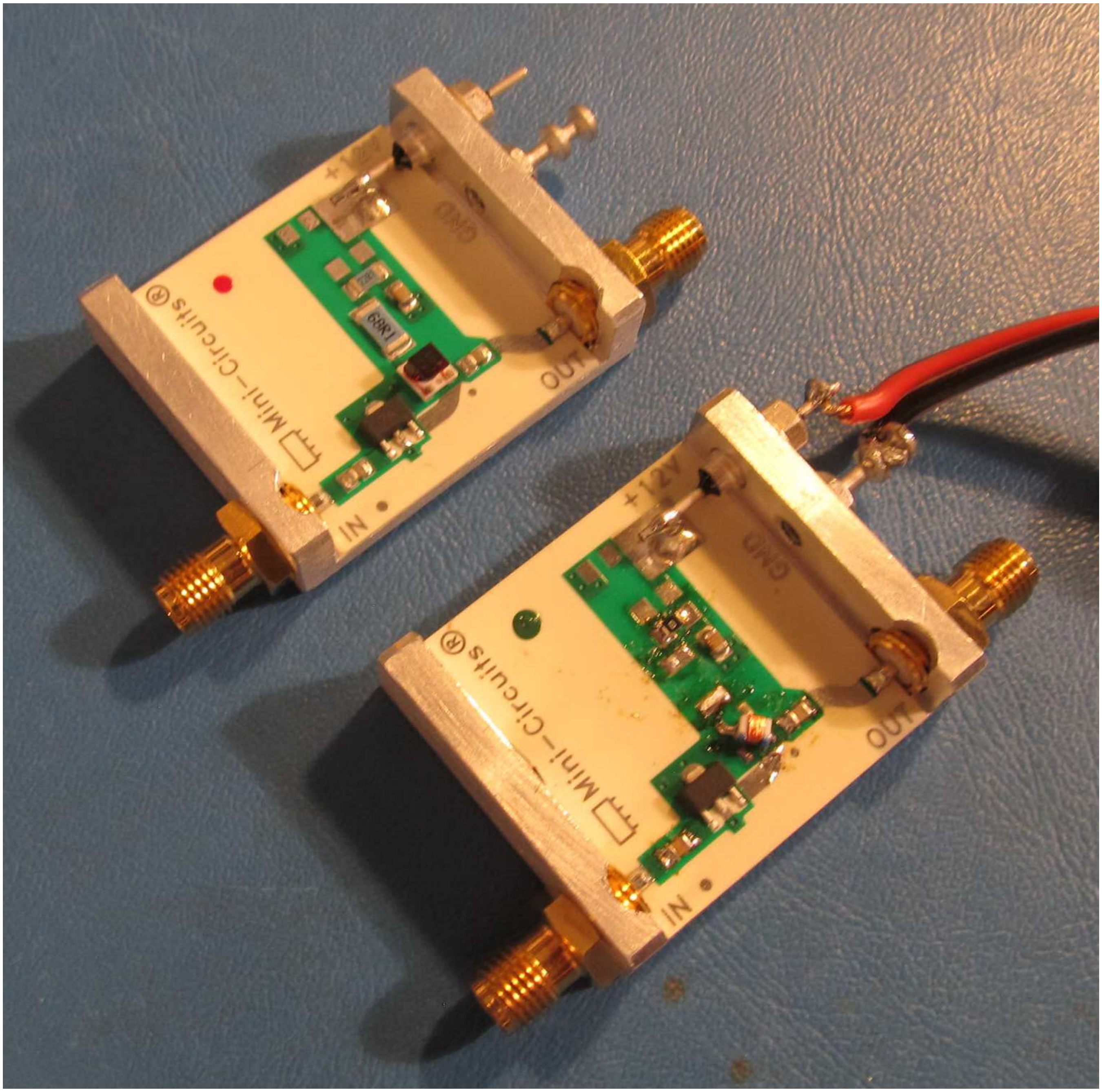
GALI-74+ Noise Figure for each supply voltage. Note exaggerated vertical scale.

<u>1 dB compression</u>: The GALI-74+ datasheet specifies a minimum output power of +18 dBm for 1 dB compression. Assuming 25 dB amplifier gain, the input would be –6 dBm minimum. In all cases, the 1 dB compression point was reached with a higher input level of about –4.7 to –4.5 dB. The compression measurements were made at a single frequency of 40 MHz, approximately mid-band for the LWA. Measurements were made at the input levels of –50, –30, –20 and –16 dBm and above –16 dBm in 1 dB increments up to –4 dBm. The measurements showed linear amplifier operation (within a couple hundredths of a dB) at all supply voltages and device input powers up to of approximately –8 dBm at which point the output started to compress slightly. With an input power of –4 dBm, the output compression level decreased 0.16 dB from 1.35 dB at 7.3 V supply voltage to 1.19 dB at 12.0 V supply voltage. See plot below.



GALI-74+ 1 dB Compression for each supply voltage. The orange arrows point to the 1 dB compression points.

Appendix ~ Mini-Circuits TB-409-74+ Evaluation Board Before (upper) & After (lower) Bias-Tee Modification



Document Information

Author: Whitham D. Reeve

Revisions: 0.0 (Original draft started, 15 Apr 2023)

0.1 (Completed all measurements and added data, 19 Apr 2023)

0.2 (Added images and minor text edits, 20 Apr 2023)

0.3 (Distribution, 28 Aug 2023)

0.4 (Added Coilcraft p/n and before/after images of evaluation board, 03 Oct 2023)

Word count: 1524

File size (bytes): 3149750

Memo Cover Sheet

ARX-Eval-07

Monitoring Components Evaluation
15 October 2023
Whitham D. Reeve

Monitoring Components Evaluation

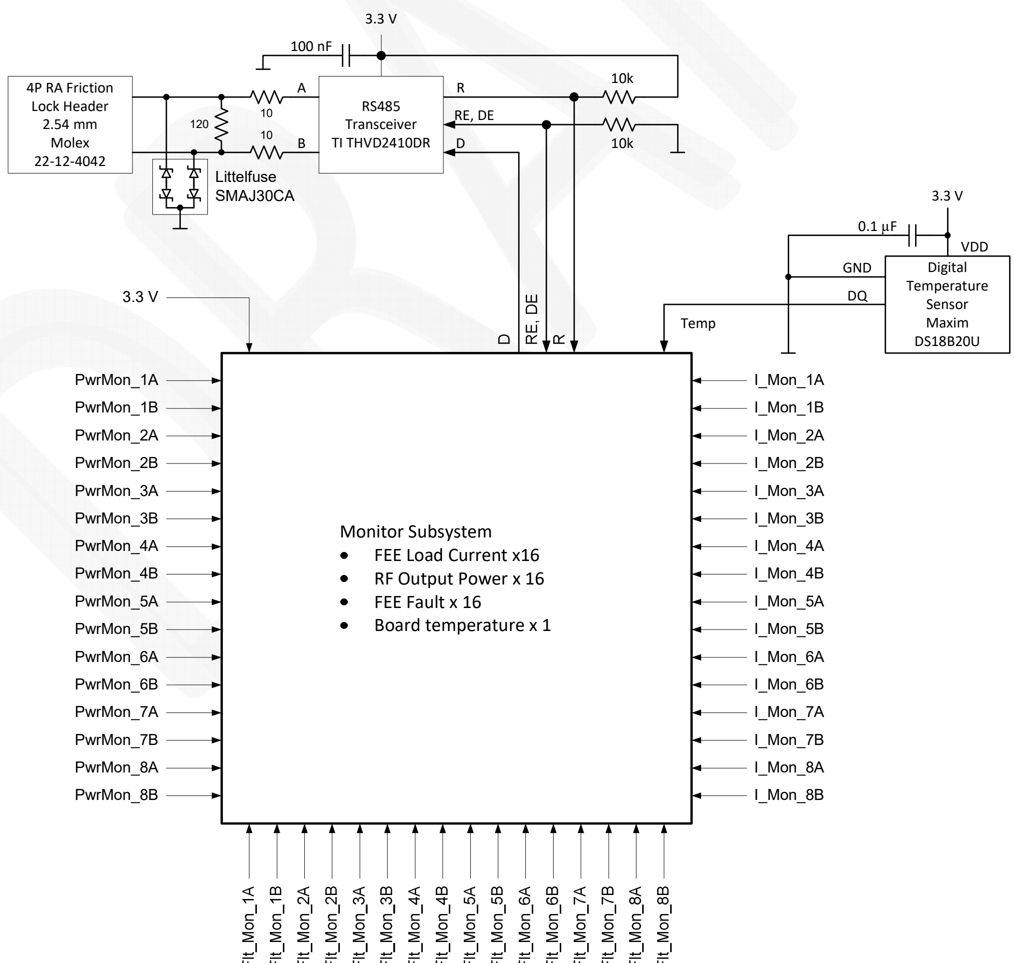
This document provides analyses of the monitoring components used in the existing Rev. G and H ARX and proposed for use in the Rev. I ARX. Refer to the Rev. I ARX block diagram for reference (see Reports folder).

Monitor Subsystem:

<u>Monitoring components</u>: The Rev. G ARX has no specific monitors or diagnostics, whereas the Rev. H ARX has a microprocessor controlled FEE load current monitor and RF output power detector and used the EIA-485 interface for communications.

The Rev. I ARX borrows the basic monitor concepts from the Rev. H ARX but uses the Serial Peripheral Interface (SPI) for communications; this SPI is separate from the SPI used to control the ARX. The Rev. I monitor subsystem provides microprocessor controlled monitoring of at least 49 signals (see basic monitor subsystem block diagram below):

- ✓ FEE load current (signal from the TI TPS16412 eFuse): 16 analog monitor points;
- ✓ FEE fault (signal from the TI TPS16412 eFuse): 16 digital monitor points;
- ✓ RF output power (signal from the ADI AD8361 detector IC): 16 analog monitor points;
- ✓ Board temperature: At least 1 analog monitor point.



To minimize the possibility of self-generated radio frequency interference (RFI), the microprocessor is activated only for diagnostic purposes and powered down at all other times. The monitor subsystem including microprocessor, FEE fault indication, temperature and associated analog signals (FEE load current and RF output power) is operated through a separate TIA-485 control interface. All analog signals are single-ended.

The Rev. H ARX uses the PIC16F15386-E_PT microcontroller, and it is proposed to use the same PIC in the Rev. I ARX for compatibility with existing control system hardware and software.

TIA-485 Interface:
The TIA-485 (commonly called RS-485) interface is used to communicate with the Monitor Subsystem. The Rev. H ARX uses the half-duplex, 500 kbps Texas Instruments THVD1500DR transceiver IC, but it only works with a 5 V power supply. The Rev. I uses the TI THVD2410DR IC, which operates from 3 to 5.5 V and otherwise has similar performance.

TI recommends the component values shown in the schematic below. The 120 ohm resistor across A and B terminates the transmission line. The two 10 ohm resistors in series with A and B limit short-circuit current. The Littelfuse SMAJ30CA TVS connected from A and B to ground has a 30 V working voltage.

Temperature Monitor:
At least one temperature sensor will be placed on the Rev. I ARX PCB. Additional details including its location on the PCB will be provided in this section as they are developed.

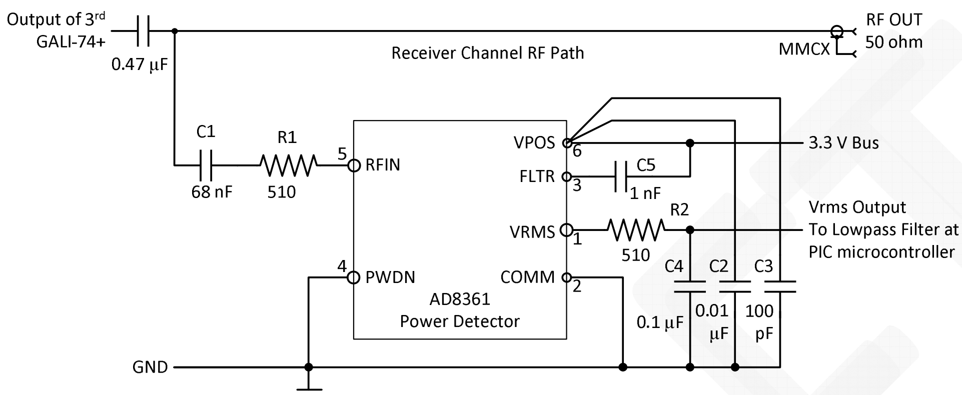
The Rev. H ARX uses the Maxim DS18B20U digital temperature sensor. It is assumed that precise temperature is not needed for diagnostics.

ARX FEE Current and Fault Monitor:
The Rev. I ARX uses a TPS16412 eFuse to control power to each FEE. The eFuse produces an output voltage to the monitor subsystem that is proportional to the load current. It also produces an overcurrent fault indication that drives a low-current LED on the PCB and an output to the monitor subsystem. Refer to ***Evaluation of the TI TPS16412 eFuse for Use in the Rev. I ARX*** for additional information about the eFuse. Additional details concerning the eFuse connections to the monitor subsystem will be provided in this section as they are developed.

ARX RF Output Power Detector:
Device type: The Rev. H ARX uses the SOT-23 version of the AD8361 power detector IC. The same basic design is incorporated in the Rev. I ARX with only a change in the input capacitor as described below. The device RF input is the total power in the passband spectrum, which depends on the ARX filter settings but in the worst-case will be on the order of 100 MHz wide. The power detector has an internal squaring functions and filter that produces a dc voltage output that is proportional to the square root of the average, or rms, value of input voltage.

The dynamic range of the AD8361 is specified in the datasheet only for CW signals and is given as 26 to 30 dB depending on the error. An error of a few dB can be expected at low levels of around 20 mVrms, or -21 dBm; the error rapidly increases at lower input signal levels. The actual ARX signals generally are noise-like, but the dynamic range of the power detector in the ARX application probably is not much different since the device responds to the rms voltage on its input.

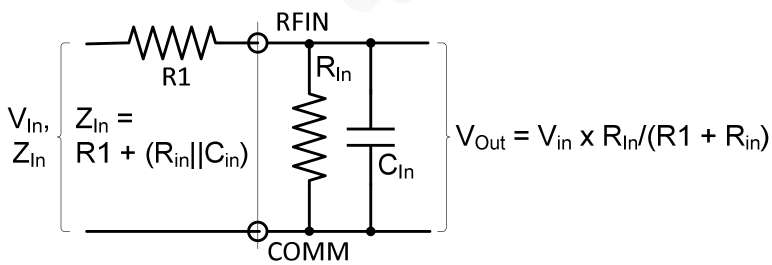
AD8361 Application Schematic:



Device connections: The datasheet mentions in several places that two power supply decoupling capacitors, C2 and C3 in the schematic, are used. The datasheet also provides guidance on controlling the input interface impedance for a 50 ohm system but, in the ARX application, the AD8361 is connected to the RF path through a relatively high-impedance bridging connection and appears as shunt load across the 50 ohm RF path.

The RF power detector output is a dc voltage but is curiously named Vrms in the datasheet. It is connected to an ADC channel in a Monitor Subsystem (see previous section) through lowpass filters. The RF input and dc output are further discussed below.

RF Input: Refer to the full schematic above. C1 is required to isolate the RF path from the dc voltage on the device's RFIN pin. Its capacitance is large enough to provide negligible impedance to the RF signal. C1 = 2 nF in the Rev. H design. C1 = 68 nF in the Rev. I design for commonality with other isolation capacitors in the receiver channel. The impedance of 68 nF is –j0.78 ohms at 3 MHz. R1 forms a voltage divider with the device input impedance of 225 ohms in parallel with 0.9 pF capacitance (see equivalent circuit below). The value of R1 is a tradeoff between providing a high input signal voltage (low resistance) and a high bridging impedance (high resistance).



The capacitive reactance of Cin at 100 MHz is –j1768 ohms, and the impedance magnitude of the parallel combination of RIN and Cin is 223 ohms. Thus, the impedance seen by the RF path to which this circuit is bridged is approximately R1 + 223 ohms.

In the Rev. H ARX, R1 = 510 ohms, so the shunt impedance on the RF path is R1 + RIN, or about 733 ohms. The impedance seen by the RF path at its junction with the bridging circuit is the parallel combination of 50 ohms and 733 ohms, or 46.8 ohms. This is an impedance change of –6.4%, and the return loss seen by the 50 ohm RF path is 29.6 dB. The voltage drop factor with R1 = 510 ohms and RIN = 223 ohm input impedance is approximately 0.30, or –10.3 dB. Therefore, for R1 = 510 ohms, the AD8361 sensitivity is reduced by 10.3 dB. For reference, the series resistance R1 for any desired input attenuation can expressed as

$R1 = RIN\,(1 - 10^{ATTN/20})/(10^{ATTN/20})$

where *RIN* is the device input impedance (223 ohms) and *ATTN* is the desired attenuation in dB.

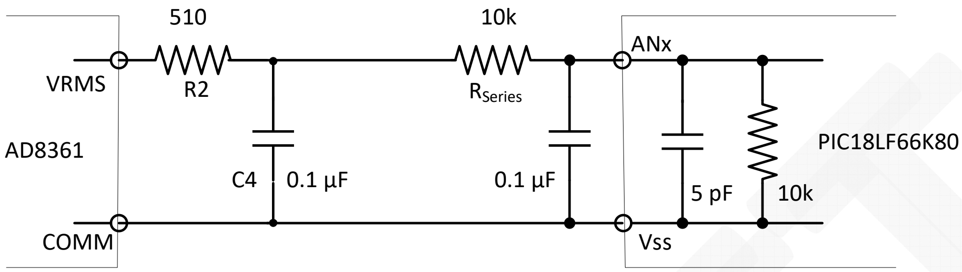
If it is desired to introduce no more than 2% impedance change at the junction, the value of R1 would have to be about 2500 ohms. If R1 = 2500 ohms, the equivalent return loss is 39.9 dB, and improvement of 10.3 dB compared to R1 = 510 ohms. The volage drop factor when R1 = 2500 ohms is approximately 0.08, or –21.7 dB. Thus, while R1 = 2500 ohms improves the impedance mismatch of the bridging connection, it decreases the voltage available at the output of the power detector, and thus the device sensitivity, by 10.4 dB compared to R1 = 510 ohms.

The AD8361 loses accuracy at low input signal levels so, depending on the normal signal levels being monitored, a decrease of 10.4 dB compared to the Rev. H ARX may be a significant reduction of the power detector performance. There have been no reports of unsatisfactory operation of the power detector with R1 = 510 ohms. Therefore, no changes are made to the input series resistor in Rev. I compared to the Rev. H design.

<u>Signal input range</u>: The SOT-23 version of the AD8361 operates in the ground-reference mode in which its output is referenced to 0 V. The upper input limit for a linear response when operated from a 3.3 V power supply typically is 390 mVrms. In a 50 ohm system, this voltage is equivalent to +4.8 dBm at the device's signal input interface. However, the device input impedance is 225 ohms in parallel with a 0.9 pF capacitor at the frequencies of interest (< 100 MHz) and, as discussed above, a 510 ohm resistor is placed in series with the input, which increases the overall input impedance at the RF path measurement point to about 733 ohms. Therefore, with the voltage divider used in the ARX application, the input voltage limit of 390 mVrms at the RFIN pin corresponds to 1.28 Vrms at the RF path connection. This is equivalent to a power level in the 50 ohm RF path of +15 dBm.

<u>External Filter Capacitor</u>: The power detector has an internal lowpass filter for reducing ripple on its output. It consists of 27 pF || 2 kohms for small input signals. As the input signal increases, the resistive component decreases. For large input signals, the filter is equivalent to 27 pF || 500 ohms. The associated RC corner frequencies for small and large input signals are 3 and 12 MHz, respectively. Connecting an external capacitor between the FLTR pin and VPOS reduces the corner frequency. The Rev. H ARX uses a 1 nF external filter capacitor with corresponding small and large signal corner frequencies of 77 and 310 kHz, respectively. This capacitor value appears to be adequate and is proposed for the Rev. I ARX.

Output Termination and Filtering: The Rev. H ARX has an RC lowpass filter consisting of a series 510 ohm resistor and 0.1 µF shunt capacitor connected closely to the AD8361 output. The corner frequency of this combination is 31 kHz. This filter is then connected to RSeries = 10 kohms series resistor and 0.1 µF capacitor close to the PIC ADC input, and its corner frequency is 159 kHz. The PIC18LF66K80 datasheet recommends a source impedance of 10 kohms, which is satisfied by RSeries shown below. The purpose of the first filter (R2, C4) is not known, but it is not changed in the Rev. I ARX.



Document Information

Author: Whitham D. Reeve

Revisions: 0.0 (Original draft started based on logic evaluation document, 29 Sep 2023)

0.1 (Added AD8361 power detector, 11 Oct 2023)

0.2 (Updated AD8361 output schematics, 13 Oct 2023)

0.3 (Revised Monitor Subsystem block diagram and added sections, 14 Oct 2023)

0.4 (Updated AD8361 application schematic & discussion, 15 Oct 2023)

Word count: 1807

File size (bytes): 74352

Memo Cover Sheet

ARX-Eval-08

ARX PCB Stackup Evaluation

7 December 2023

Whitham D. Reeve

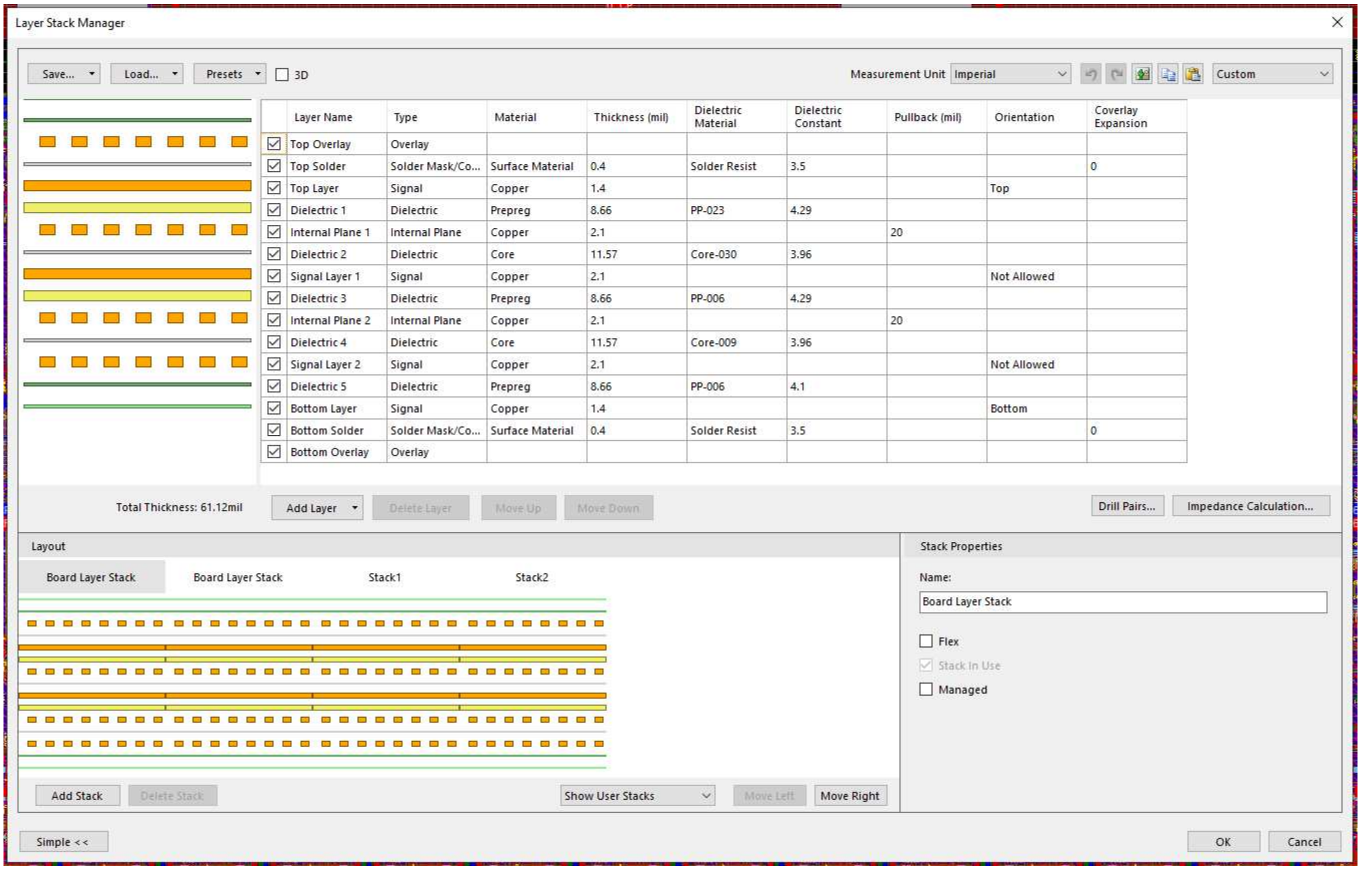
Board Stackup Evaluation

PCB Layering:

The Rev. F (and presumably G) uses a 4-layer PCBs and Rev. H uses a 6-layer. Because of the need for diagnostics and associated routing, a 6-layer PCB will be used for Rev. I, similar to Rev. H.

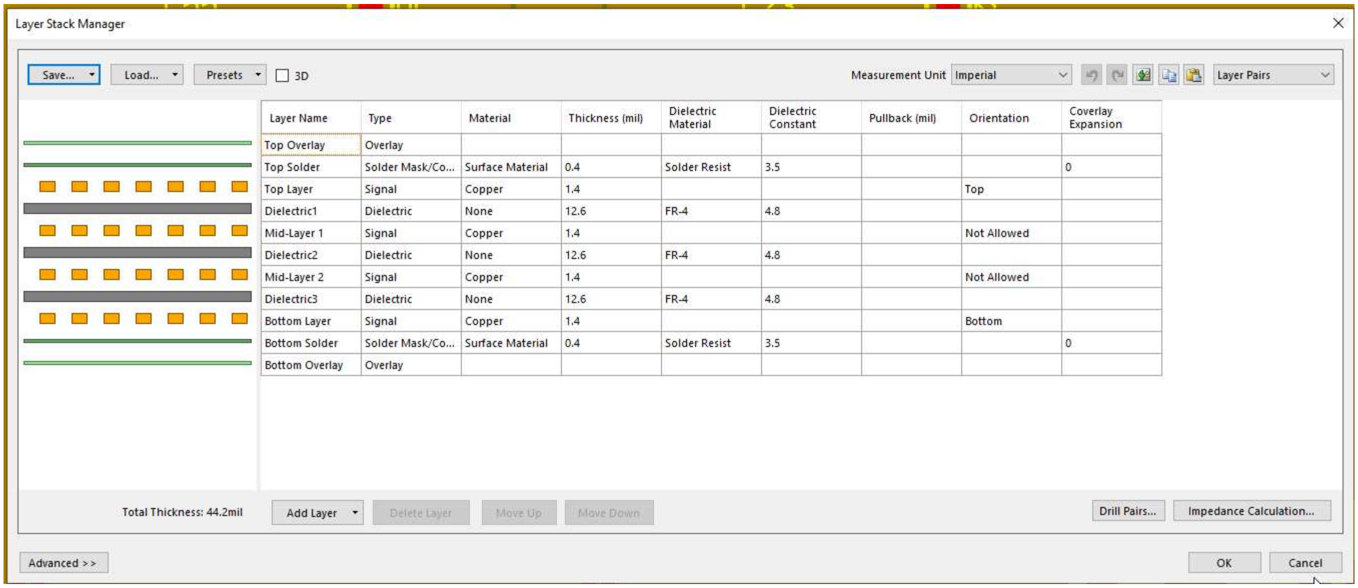
Stackup comparison:

The Rev. H stackup is shown below based on the Altium files.



Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant	Pullback (mil)	Orientation	Coverlay Expansion
Top Overlay	Overlay							
Top Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5			0
Top Layer	Signal	Copper	1.4				Top	
Dielectric 1	Dielectric	Prepreg	8.66	PP-023	4.29			
Internal Plane 1	Internal Plane	Copper	2.1			20		
Dielectric 2	Dielectric	Core	11.57	Core-030	3.96			
Signal Layer 1	Signal	Copper	2.1				Not Allowed	
Dielectric 3	Dielectric	Prepreg	8.66	PP-006	4.29			
Internal Plane 2	Internal Plane	Copper	2.1			20		
Dielectric 4	Dielectric	Core	11.57	Core-009	3.96			
Signal Layer 2	Signal	Copper	2.1				Not Allowed	
Dielectric 5	Dielectric	Prepreg	8.66	PP-006	4.1			
Bottom Layer	Signal	Copper	1.4				Bottom	
Bottom Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5			0
Bottom Overlay	Overlay							

Although it will not be used, the Rev. F stackup is shown below for reference.



Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant	Pullback (mil)	Orientation	Coverlay Expansion
Top Overlay	Overlay							
Top Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5			0
Top Layer	Signal	Copper	1.4				Top	
Dielectric1	Dielectric	None	12.6	FR-4	4.8			
Mid-Layer 1	Signal	Copper	1.4				Not Allowed	
Dielectric2	Dielectric	None	12.6	FR-4	4.8			
Mid-Layer 2	Signal	Copper	1.4				Not Allowed	
Dielectric3	Dielectric	None	12.6	FR-4	4.8			
Bottom Layer	Signal	Copper	1.4				Bottom	
Bottom Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5			0
Bottom Overlay	Overlay							

Rev. I PCB manufacturing:

JLCPCB manufactured the PCBs for Filter Evaluation and the products were satisfactory, so they were investigated for manufacturing the ARX Rev. I prototype PCBs. The PCBs will be 6-layer, 1.6 mm thick with 1 oz copper on the outer layers and 2 oz copper on the inner layers. JLCPCB has only one “Impedance Controlled” 6-layer stackup for the required configuration as shown below. Note that the “No requirement stackup” is identical to the “JLC061612-1080 stackup”.

6-Layer Impedance Control Stackup

Thickness: 1.2mm | 1.6mm | 2.0mm

Outer Copper Weight: 1oz | 2oz

inner Copper Weight: 0.5oz | 1oz | 2oz

1) No requirement Stackup

Layer	Material Type	Thickness	
Layer	Copper	0.035mm	
Prepreg	1080*1	0.084mm	
Prepreg	1080*1	0.0535mm	
inner Layer	Copper	0.061mm	
Core>	Core	0.35mm	0.35mm (with copper core)
inner Layer	Copper	0.061mm	
Prepreg	1080*1	0.0535mm	
Prepreg	2116*1	0.124mm	
Prepreg	1080*1	0.0535mm	
inner Layer	Copper	0.061mm	
Core>	Core	0.35mm	0.35mm (with copper core)
inner Layer	Copper	0.061mm	
Prepreg	1080*1	0.0535mm	
Prepreg	1080*1	0.084mm	
Layer	Copper	0.035mm	

2) JLC061612-1080 Stackup

Layer	Material Type	Thickness	
Layer	Copper	0.035mm	
Prepreg	1080*1	0.084mm	
Prepreg	1080*1	0.0535mm	
inner Layer	Copper	0.061mm	
Core>	Core	0.35mm	0.35mm (without copper core)
inner Layer	Copper	0.061mm	
Prepreg	1080*1	0.0535mm	
Prepreg	2116*1	0.124mm	
Prepreg	1080*1	0.0535mm	
inner Layer	Copper	0.061mm	
Core>	Core	0.35mm	0.35mm (without copper core)
inner Layer	Copper	0.061mm	
Prepreg	1080*1	0.0535mm	
Prepreg	1080*1	0.084mm	
Layer	Copper	0.035mm	

Comparison of Rev. H ARX 6-layer stackup with JLCPCB 6-layer stackup:

Rev. H							**JLCPCB**	**JLC061612-1080 Stackup**		
Layer name	**Type**	**Material**	**Thickness (mil)**	**Dielectric material**	**Dielectric constant**		**Layer**	**Material**	**Thickness (mil)**	**Dielectric constant**
Top overlay	Overlay									
Top solder	Soldermask	Surface material	0.4	Solder resist	3.5		Coating	C2	0.6	3.8
Top layer	Signal	Copper	1.4				Signal	Copper	1.38	
Dielectric 1	Dielectric	Prepreg	8.66	PP-023	4.29		Dielectric	Prepreg	5.4	3.91
Internal plane 1	Internal plane	Copper	2.1				Internal plane	Copper	2.4	
Dielectric 2	Dielectric	Core	11.57	Core-030	3.96		Dielectric	Core	13.78	4.6
Signal layer 1	Signal	Copper	2.1				Signal	Copper	2.4	
Dielectric 3	Dielectric	Prepreg	8.66	PP-006	4.29		Dielectric	Prepreg	9.1	3.91 + 4.16 + 3.91
Internal plane 2	Internal plane	Copper	2.1				Internal plane	Copper	2.4	
Dielectric 4	Dielectric	Core	11.57	Core-009	3.96		Dielectric	Core	13.78	4.6
Signal layer 2	Signal	Copper	2.1				Signal	Copper	2.4	
Dielectric 5	Dielectric	Prepreg	8.66	PP-006	4.1		Dielectric	Prepreg	5.4	3.91
Bottom layer	Signal	Copper	1.4				Signal	Copper	1.38	
Bottom solder	Soldermask	Surface material	0.4	Solder resist	3.5		Coating	C2	0.6	3.8
Bottom overlay	Overlay									
		Total thickness	**61.12**					**Total thickness**	**61.02**	

Document Information

Author: Whitham D. Reeve

Revisions: 0.0 (Original draft started, 07 Dec 2023)

Word count: 357

File size (bytes): 2489429

Memo Cover Sheet

ARX-Eval-09

RF Switch & Digital Step Attenuator Evaluation

30 January 2024

Whitham D. Reeve

RF Switch & Digital Step Attenuator Evaluation

Whitham D. Reeve

This document provides analyses of the RF switches and digital step attenuators used in the existing Rev. G and H ARX and proposed for use in the Rev. I ARX. Refer to the Rev. I ARX System Block Diagram in the Reports folder. Also included is a brief summary of how the RF switches were found and analyzed.

<u>RF switch</u>: The Rev. G ARX used the Macom MASWSS-0115 SPDT reflective switch for the split and reduced bandwidth filters and the Hittite (ADI) HMC245QS16E SP3T absorptive switch for the 3 and 10 MHz HPF. The Rev. H ARX used the Peregrine Semiconductor (pSemi) PE42422 SPDT switch for both the HPF and LPF.

The Rev. I ARX is proposed to use the Analog Devices HMC-194A SPDT and P-Semi PE42540 SP4T switches. See table below for a comparison. The proposed Rev. I switches are shown shaded.

ARX Revision	**Rev. I**	**Rev. I**	**Rev. G**	**Rev. G**	**Rev. H**
Type	**SPDT**	**SP4T**	**SPDT**	**SP3T**	**SPDT**
Parameter	**HMC 194A**	**PE42540**	**MASWSS-0115**	**HMC245QS16E**	**PE42422**
Voltage (V)	3.3 V	3.3 V	3 V	5 V	2.3 – 5 V
Freq Low (MHz)	dc	10 Hz	dc	dc	dc
Freq Hi (MHz)	3 GHz	8 GHz	3 GHz	3.5 GHz	6 GHz
IL (dB)	0.5/0.9 max	0.80/1.1 max	0.25/0.40 max	0.70/1.0 max	0.23 typ
ISO (dB)	50 min/55	45/40 min	20 min	46/40 min	68 typ
RL (dB)	26 typ	23 typ	20 typ	23 typ	33 typ
1 dB (dBm)	24 min28 typ	33/31 min	21/25 typ	29/26 min	33 typ
IP2 (dBm)	N/A	100 typ	90 typ	N/A	96/105 typ
IP3 (dBm)	40 min/53 typ	58 typ	45 typ	48/44 min	75/81 typ
Cost (100 pc)	$3.28	$9.35	$1.10	$7.19	$1.61

An important concern is the switch performance under high power conditions including the 1 dB compression and 2nd and 3rd order intercept points. The proposed HMC-194A SPDT LPF switches are located prior to any amplification so are subject only to relatively low RF levels. The 1 dB compression point at the output of the 1st stage amplifier is +18 dBm. With an amplifier gain of 25 dB, the input would be –7 dBm for 1 dB compression. The HMC-194A SPDT switch has a minimum margin of 31 dB above this level. The GALI-74+ amplifier used in all three stages has IP3 of +38 dBm (IP2 is not specified for this amplifier). Since the amplifier IP3 is at least 2 dB lower than switch IP3, the amplifier IP3 controls.

The proposed PE42540 SP4T HPF switches are located after the 1st amplifier stage and between the 2nd digital step attenuator and the 2nd amplifier stage. Assuming the attenuator is set to 0 dB, the output of the 1st amplifier stage will be +18 dBm at its 1 dB compression point. The PE42540 SP4T switch has a minimum1 dB compression point of 31 dB, in which case the margin is 13 dB. As with IP3 above, the amplifier IP3 controls.

The relatively high gain of the receiver stages and the ability to control the attenuation in 0.5 dB steps with the digital step attenuators reduces the effects of the switch insertion losses. The cascade of two SPDT and two SP4T switches will have a maximum insertion loss of 4.0 dB.

Another important consideration is isolation between poles of the switches. High isolation is considered desirable to minimize interaction between the filters. The minimum isolation of the selected switches is 40 dB for the PE42540 and 50 dB for the HMC-194A. Return losses of the proposed switches are above 20 dB. The proposed switches are compatible with the Rev. I ARX 3.3 V bus voltage.

The total cost of a set of SPDT and SP4T switches (HMC-194A and PE42540), 2 of each switch in each ARX channel, in 100 pc quantity is $25.26.

Analyses of the RF switches proceeded as follows: The websites of the known RF switch manufacturers were searched for suitable products. The manufacturers were Analog Devices (Hittite), Macom, Mini-Circuits, and pSemi (Perregrine Semiconductor). Other manufacturers were found on distributor websites (Mouser and Digi-Key) but none met the basic requirements.

The basic requirements, in order of search filtering, were low frequency (0 to 3 MHz), operating and control voltage (3 V single supply voltage), and minimum isolation (≥ 30 dB). Some switches have a recommended supply or control voltage of 3.3 V, and I assume this can be accommodated by increasing the 3 V bus to 3.3 V. Many switches were found that require a 5 V single supply voltage, dual supply voltages (+ and -) or a negative single supply voltage, but these all were rejected. Switch packaging or parameters not shown on the spreadsheet were not used in the searches.

After filtering the results for the basic requirements, the insertion loss, cost and other parameters were tabulated. Approximately 16 SPDT switches and 4 SP4T switches were found by this method. With some exceptions, the datasheets generally specified the isolation parameter at frequencies ≥ 1 GHz or from 0 to 1 GHZ or 0 to 2.5 GHz and not specifically at the lower frequencies of interest (< 100 MHz).

The isolation vs frequency plots for some switches with isolation < 30 dB also were viewed. Some switches in this category had much higher isolation at the lower frequencies but most plots showed little detail or were useless below 500 MHz. Also, these plots were typical and not minimum.

The difference between typical and minimum is on the order of 10 dB, more or less, but this can vary with the manufacturer and product. This means that the switch isolation at the frequencies of interest becomes somewhat subjective and generally best verified by a manufacturer's evaluation module or board. However, due to cost, availability and the time required to design and perform evaluation tests, I did not do this for any of the RF switches.

Addendum added 30 Jan 2024 for RF switch modifications:
The filter output switches are rotated 180° with respect to the input switches on the PCB. To prevent crossing the filter RF traces and having to use vias, the ports to which the filters are connected on the output are not one-to-one; that is, the filter on RF1 on the input switch is not connected through a filter to RF1 on the output switch. Instead, the filter on RF1 on the input switch is connected through a filter to RF2 on the output switch, and so on. This required changes in the truth tables for the output switch shown below.

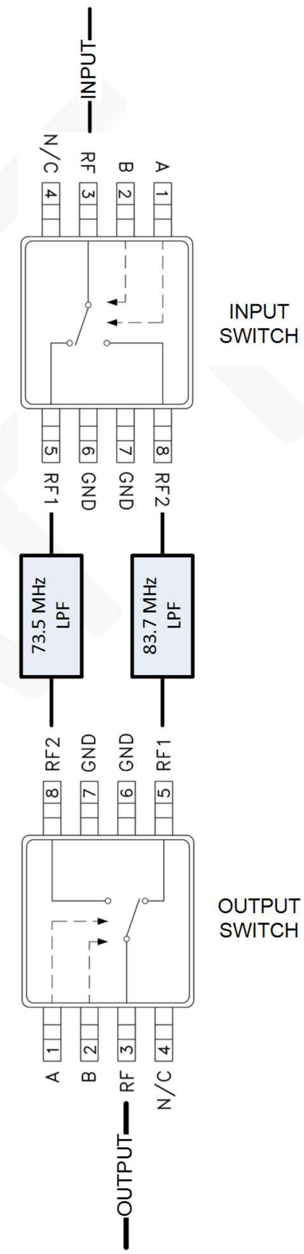
SPDT RF Switch ADI HMC194A Logic

Table 1 ~ Original logic:

Direction	A B	Switch
IN 73.5 MHz	0 1	RF1 – IN
OUT 73.5 MHz	0 1	RF1 – OUT
IN 83.7 MHz	1 0	RF2 – IN
OUT 83.7 MHz	1 0	RF2 – OUT

Table 2 ~ Inverted logic:
A & B reversed on output switch

Direction	A B (orig)	Switch
IN 73.5 MHz	0 1 (0 1)	RF1 – IN
OUT 73.5 MHz	1 0 (0 1)	RF2 – OUT
IN 83.7 MHz	1 0 (1 0)	RF2 – IN
OUT 83.7 MHz	0 1 (1 0)	RF1 – OUT



SP4T RF Switch P-Semi 42540 Logic

Table 1 ~ Original logic:

Direction	V1 V2	Switch
IN 3 MHz	0 0	RF1 – IN
OUT 3 MHz	0 0	RF1 – OUT
IN 10 MHz	1 0	RF2 – IN
OUT 10 MHz	1 0	RF2 – OUT
IN 20 MHz	0 1	RF3 – IN
OUT 20 MHz	0 1	RF3 – OUT
IN 30 MHz	1 1	RF4 – IN
OUT 30 MHz	1 1	RF4 – OUT

Table 2 ~ Inverted logic:
V1 inverted on output switch

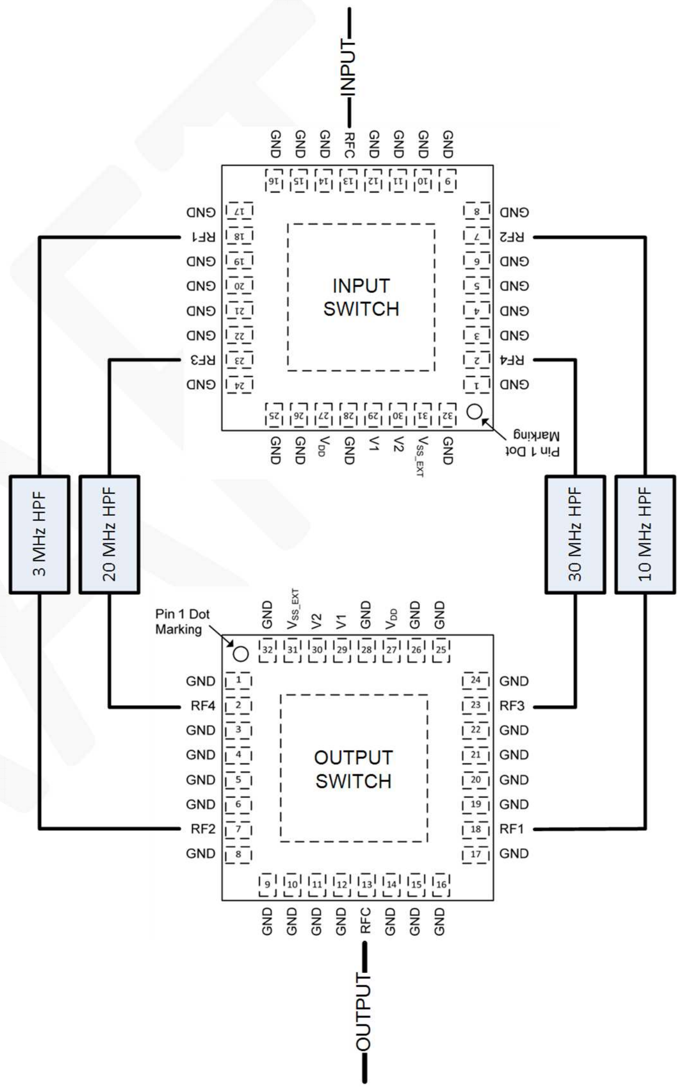
Direction	V1 V2 (orig)	Switch
IN 3 MHz	0 0 (0 0)	RF1 – IN
OUT 3 MHz	1 0 (0 0)	RF2 – OUT
IN 10 MHz	1 0 (1 0)	RF2 – IN
OUT 10 MHz	0 0 (1 0)	RF1 – OUT
IN 20 MHz	0 1 (0 1)	RF3 – IN
OUT 20 MHz	1 1 (0 1)	RF4 – OUT
IN 30 MHz	1 1 (1 1)	RF4 – IN
OUT 30 MHz	0 1 (1 1)	RF3 – OUT

Table 3 ~ Inverted logic:
V2 inverted on output switch only

Direction	V1 V2 (orig)	Switch
IN 3 MHz	0 0 (0 0)	RF1 – IN
OUT 3 MHz	0 1 (0 0)	RF3 – OUT
IN 10 MHz	0 1 (0 1)	RF3 – IN
OUT 10 MHz	0 0 (0 1)	RF1 – OUT
IN 20 MHz	1 0 (1 0)	RF2 – IN
OUT 20 MHz	1 1 (1 0)	RF4 – OUT
IN 30 MHz	1 1 (1 1)	RF4 – IN
OUT 30 MHz	1 0 (1 1)	RF2 - OUT

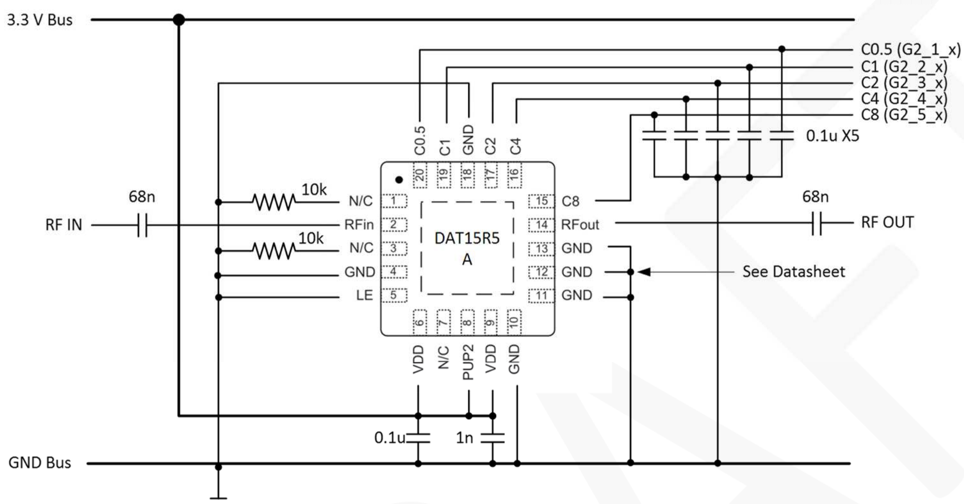
Table 4 ~ Inverted logic:
V1 & V2 inverted on output switch

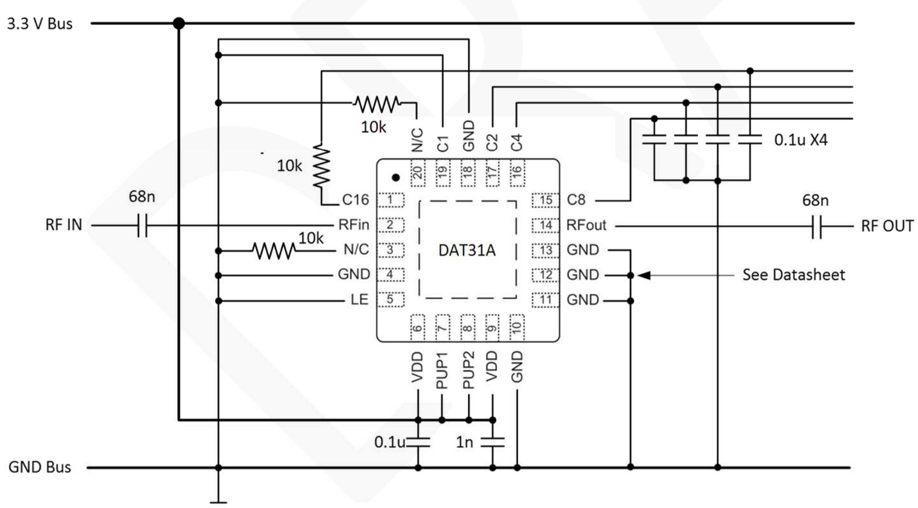
Direction	V1 V2 (orig)	Switch
IN 3 MHz	0 0 (0 0)	RF1 – IN
OUT 3 MHz	1 1 (0 0)	RF4 – OUT
IN 10 MHz	0 1 (0 1)	RF3 – IN
OUT 10 MHz	1 0 (0 1)	RF2 – OUT
IN 20 MHz	1 0 (1 0)	RF2 – IN
OUT 20 MHz	0 1 (1 0)	RF3 – OUT
IN 30 MHz	1 1 (1 1)	RF4 – IN
OUT 30 MHz	0 0 (1 1)	RF1 – OUT



<u>Digital step attenuator</u>: The Rev. G ARX used the Mini-Circuits (MCL) DAT-31A-PP+, 5 bit, 0 – 31 dB attenuators but only 4 bits were used for control, giving a 2 dB resolution. The Rev. H ARX used the Hittite HMC472ALP4E, 6 bit, 0 – 31.5 dB attenuators. The Rev. I ARX will use the DAT-31A-PP+, 5 bit, 0 – 31 dB attenuator for positions AT1 and AT2 and the DAT-15R5A-PP+, 5 bit, 0 – 15.5 dB attenuator for the third position AT3. AT1 and AT2 will continue using 4 bits for control, while AT3 will use all 5 bits for control, the latter providing 0.5 dB resolution. The MCL DAT-series attenuators are well proven in the Rev. G ARX and no special analysis is undertaken here.

Wiring and connection considerations taken from the MCL datasheets are shown below.





Document Information

Author: Whitham D. Reeve

Revisions: 0.0 (Original draft started, 23 Apr 2023)

0.1 (Minor edits for clarity, 24 Apr 2023)

0.2 (Updated SPDT to HMC-194A and SP4T to PE42540, added attenuator schematics, 29 Sep 2023)

0.3 (Distribution, 30 Sep 2023)

0.4 (Imported RF Switch Modifications, 30 Jan 2024)

Word count: 1185

File size (bytes): 125410

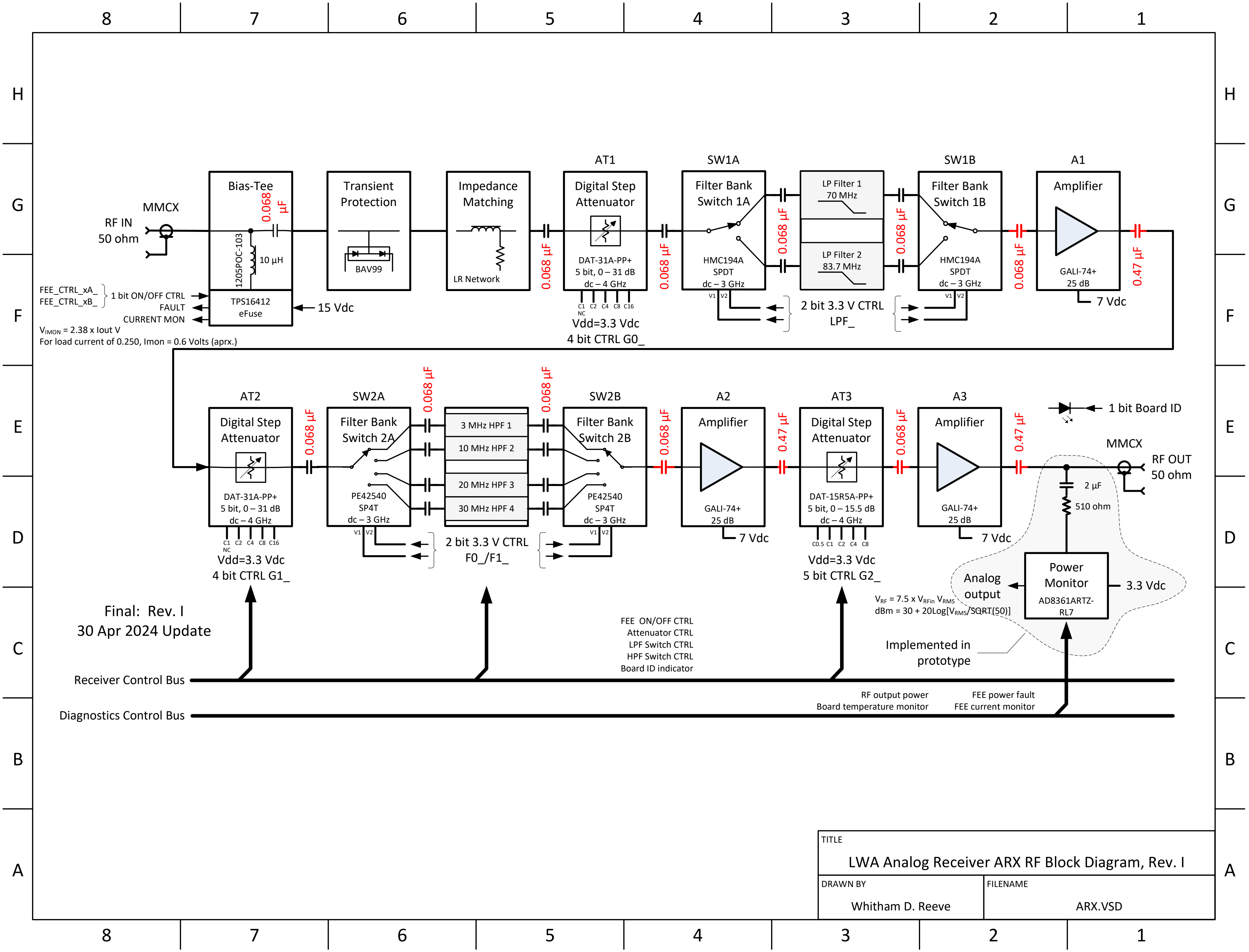
Memo Cover Sheet

ARX-Eval-10

ARX System Block Diagram

20 April 2024

Whitham D. Reeve



MMCX
RF IN
50 ohm
Bias-Tee
0.068 µF
1205POC-103
10 µH
TPS16412
eFuse
FEE_CTRL_xA_
FEE_CTRL_xB_
1 bit ON/OFF CTRL
FAULT
CURRENT MON
V_{IMON} = 2.38 x Iout V
For load current of 0.250, Imon = 0.6 Volts (aprx.)
15 Vdc
Transient Protection
BAV99
Impedance Matching
LR Network
0.068 µF
AT1
Digital Step Attenuator
DAT-31A-PP+
5 bit, 0 – 31 dB
dc – 4 GHz
C1 NC C2 C4 C8 C16
Vdd=3.3 Vdc
4 bit CTRL G0_
0.068 µF
SW1A
Filter Bank Switch 1A
HMC194A
SPDT
dc – 3 GHz
V1 V2
0.068 µF
LP Filter 1
70 MHz
LP Filter 2
83.7 MHz
2 bit 3.3 V CTRL
LPF_
0.068 µF
SW1B
Filter Bank Switch 1B
HMC194A
SPDT
dc – 3 GHz
V1 V2
0.068 µF
A1
Amplifier
GALI-74+
25 dB
7 Vdc
0.47 µF
AT2
Digital Step Attenuator
DAT-31A-PP+
5 bit, 0 – 31 dB
dc – 4 GHz
C1 NC C2 C4 C8 C16
Vdd=3.3 Vdc
4 bit CTRL G1_
0.068 µF
SW2A
Filter Bank Switch 2A
PE42540
SP4T
dc – 3 GHz
V1 V2
0.068 µF
3 MHz HPF 1
10 MHz HPF 2
20 MHz HPF 3
30 MHz HPF 4
2 bit 3.3 V CTRL
F0_/F1_
0.068 µF
SW2B
Filter Bank Switch 2B
PE42540
SP4T
dc – 3 GHz
V1 V2
0.068 µF
A2
Amplifier
GALI-74+
25 dB
7 Vdc
0.47 µF
AT3
Digital Step Attenuator
DAT-15R5A-PP+
5 bit, 0 – 15.5 dB
dc – 4 GHz
C0.5 C1 C2 C4 C8
Vdd=3.3 Vdc
5 bit CTRL G2_
0.068 µF
A3
Amplifier
GALI-74+
25 dB
7 Vdc
0.47 µF
1 bit Board ID
MMCX
RF OUT
50 ohm
2 µF
510 ohm
Power Monitor
AD8361ARTZ-RL7
3.3 Vdc
Analog output
V_{RF} = 7.5 x V_{RFin} V_{RMS}
dBm = 30 + 20Log[V_{RMS}/SQRT(50)]
Implemented in prototype
Final: Rev. I
30 Apr 2024 Update
FEE ON/OFF CTRL
Attenuator CTRL
LPF Switch CTRL
HPF Switch CTRL
Board ID indicator
Receiver Control Bus
RF output power
Board temperature monitor
FEE power fault
FEE current monitor
Diagnostics Control Bus
TITLE
LWA Analog Receiver ARX RF Block Diagram, Rev. I
DRAWN BY
Whitham D. Reeve
FILENAME
ARX.VSD

Memo Cover Sheet

ARX-Eval-11

Coupling Capacitor Evaluation

Whitham D. Reeve

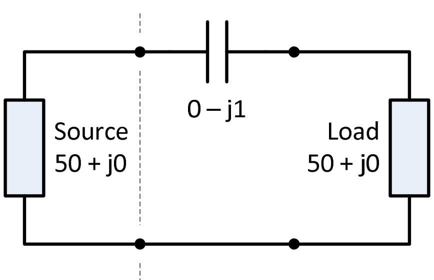
17 September 2024

Coupling Capacitor Evaluation
Whitham D. Reeve

Coupling Capacitor Application:
Coupling capacitors isolate components, such as RF switches, attenuators and RF amplifiers, from undesired dc voltages. Ideally, a coupling capacitor has reactance that decreases with frequency throughout the desired frequency range according to 1/2πfC where C is the capacitance and f is the frequency. However, practical capacitors have equivalent series resistance (ESR), equivalent series inductance (ESL), and a self-resonant frequency (SRF). The SRF is the frequency at which the capacitive reactance equals (and cancels) the inductive reactance. At the SRF, the capacitor's impedance equals the ESR and above the SRF, the capacitor has inductive reactance.

ARX Rev. G and Rev. H Coupling Capacitors:
For reference, the coupling capacitors used in the Rev. G ARX are 1000 pF (1 nF) whereas in the Rev. H ARX they are 0.1 µF (100 nF).

ARX Rev. I Requirements:
The design frequency range of the ARX is 3 to 100 MHz. The coupling capacitors are chosen to have ≤ 1 ohm impedance (≤ 2% of 50 ohms system impedance) at 3 MHz. The 1 ohm impedance is a tradeoff between large capacitors that have higher ESR and lower SRF and small capacitors with relatively high capacitive reactance that would introduce impedance mismatching at the lower frequencies.



The simple circuit shown left has 50 + j0 ohms source and load impedances and a capacitor with 0 – j1 ohms impedance (at 3 MHz) connecting them. The impedance seen by the source is 50 – J1 ohms and |Z| = 50.01 ohms. The return loss seen by the source at the junction of the source and capacitor is 40 dB, indicating that the capacitor introduces negligible impedance mismatch. If the capacitor impedance is increased to 0 – j3 ohms, |Z| = 50.09 ohms and the return loss reduces to 30.5 dB.

At higher frequencies, the capacitive reactance is (theoretically) lower and the return loss is higher. However, practical capacitors have an SRF and inductive component at higher frequencies as shown below. Ideally, for the ARX application, the capacitor SRF would be ≥ 100 MHz but this is not achievable with ordinary ceramic capacitors in the values required. The actual capacitors selected for the ARX are discussed in the next section.

<u>Selected Capacitors</u>: The theoretical reactance at 3 MHz of a 0.047 µF (47 nF) capacitor is 1.1 ohms, slightly higher than the maximum given above; therefore, a value of 0.068 µF (68 nF) is selected, which has theoretical reactance of 0.78 ohms at 3 MHz. To protect the GALI-74+ amplifiers outputs from possible transient voltage damage, 5X to 10X larger capacitors are used on the amplifier outputs as recommended in the Mini-Circuits (MCL) application note *Transient Protection of Darlington Gain Block Amplifiers*, page 10 (see References); note that these recommendations are dated 2015 and MCL did not provide a definitive answer to inquiries about the applicability of this recommendation to current GALI-74+ products. Therefore, a conservative approach is taken

to ensure there are no problems. The selected value for the amplifier output coupling capacitors is 0.47 µF (7X the input capacitor value).

Refer to the master system block diagram in the Reports folder. The Rev. I ARX RF path contains 14 coupling capacitors, 11 with 0.068 µF capacitance and 3 with 0.47 µF capacitance. The goal is to find multi-layer ceramic capacitors (MLCC) that meet the reactance requirements from 3 to 100 MHz. All capacitors are size 0805, and a tolerance of ±10% and X7R dielectric are acceptable (capacitance variation due to applied voltage is not expected to be important).

Manufacturers Evaluated:

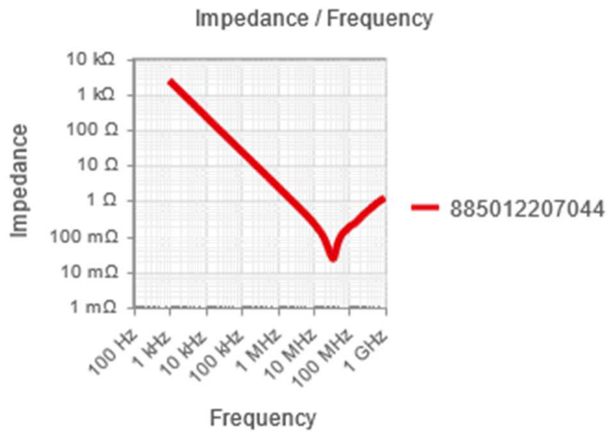
Investigation of Kemet, Kyocera, Murata, TDK and Wurth showed that all ordinary ceramic capacitors in the desired capacitance ranges have SRF far below 100 MHz. However, these capacitors still are usable if the reactance throughout the frequency range 3 to 100 MHz meets the 1 ohm requirement mentioned above; in other words, the 2% impedance requirement must be achieved throughout the entire operating frequency range even though the SRF requirement cannot be met by available parts. It is noted that if the impedance requirement is met at the 3 and 100 MHz endpoints, it will be met at all frequencies in between because the transition from capacitive to inductive reactance, and minimum impedance, occurs between the two endpoints for the capacitors being considered.

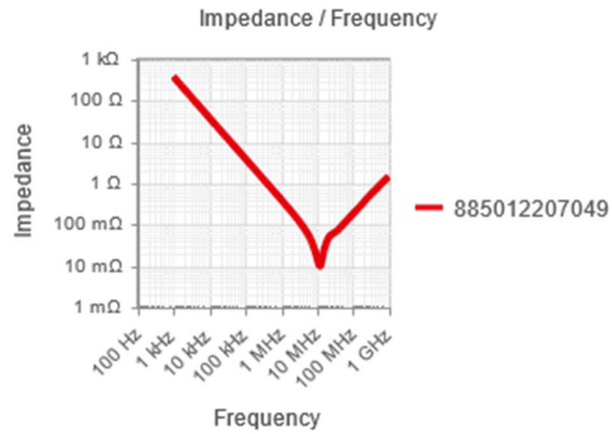
Silicon RF capacitors were investigated and rejected because of their extremely high costs. Detailed frequency-dependent data for MLCCs are available from capacitor manufacturers but, for most of them, the data are not readily accessible. TDK and Wurth Elektronik are exceptions. Wurth data, including SRF plots and other data, were the easiest to access and use through their REDEXPERT online software (see References). The analysis below is based on Wurth capacitors.

Wurth Capacitors:

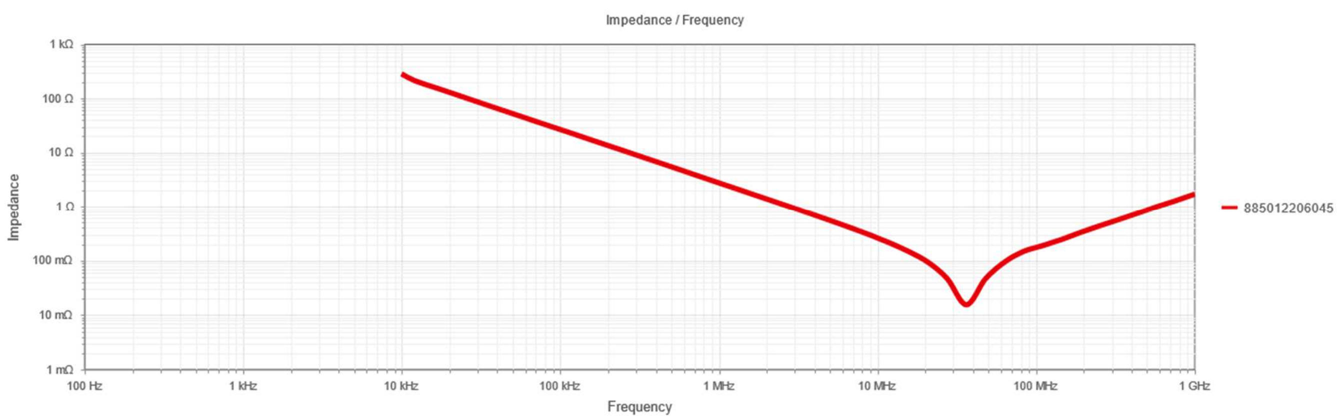
Wurth manufacturers several types of MLCCs. Its line of WCAP-CSRF High Frequency capacitors is specifically designed for RF applications but are available with a maximum value of only 33 pF. However, its line of WCAP-CSGP General Purpose capacitors reaches 47 µF in a voltage rating of 16 Vdc and a temperature rating of –55 to +125 °C.

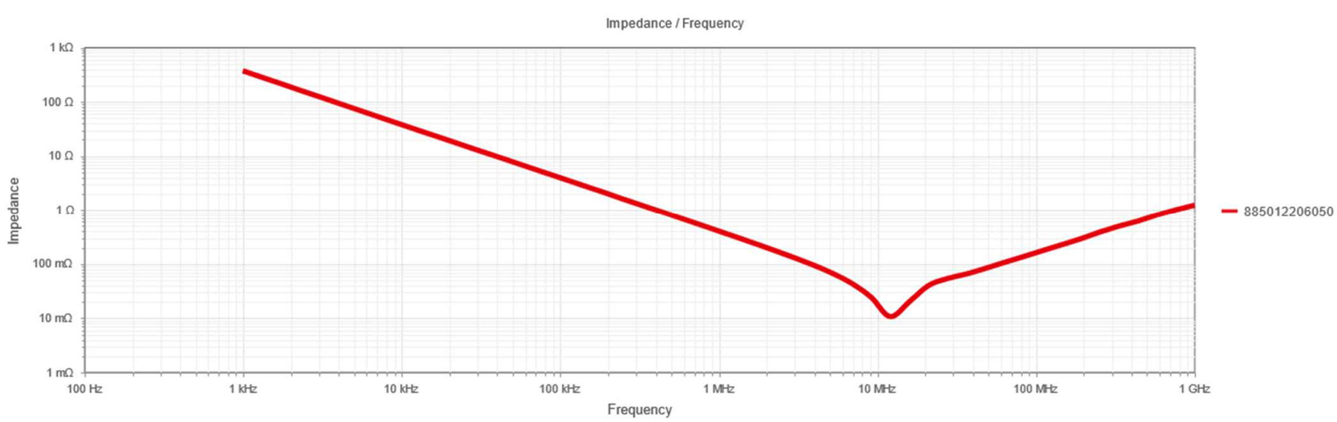
For the 0.068 µF capacitor, Wurth p/n 885012207044, the plotted impedance (below-left) is 0.845 ohms at 3 MHz and 0.181 ohms at 100 MHz. For the 0.47 µF capacitor, p/n 885012207049, the plotted impedance (below-right) is 0.129 ohms at 3 MHz and 0.176 ohms at 100 MHz. These two capacitors meet the requirements previously stated.





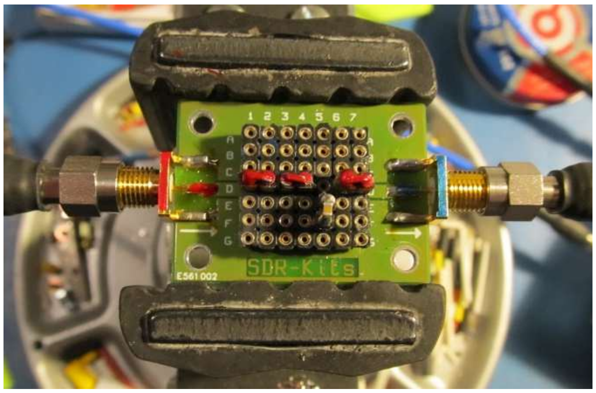
The Wurth capacitors in 0603, 16 Vdc, X7R and ±10% tolerance also were examined. These capacitors have a smaller footprint and less pad capacitance than the 0805 sizes. The plotted impedance for the 0.068 µF capacitor in 0603, p/n 885012206045 (upper image below) is 0.851 ohms at 3 MHz and 0.180 ohms at 100 MHz. For the 0.47 µF capacitor in 0603, p/n 885012206050, the plotted impedance (lower image below) is 0.124 ohms at 3 MHz and 0.165 ohms at 100 MHz. These two capacitors meet the requirements previously stated.

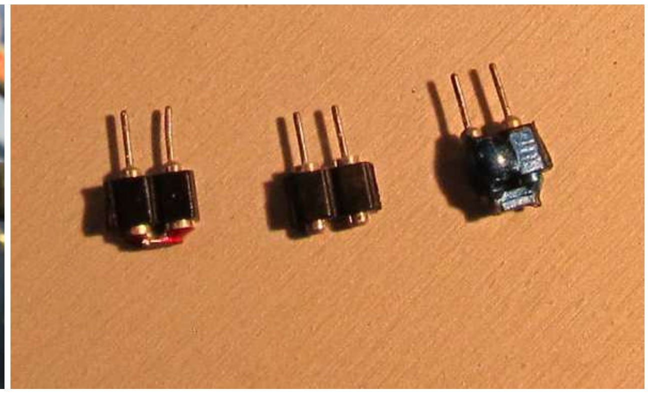




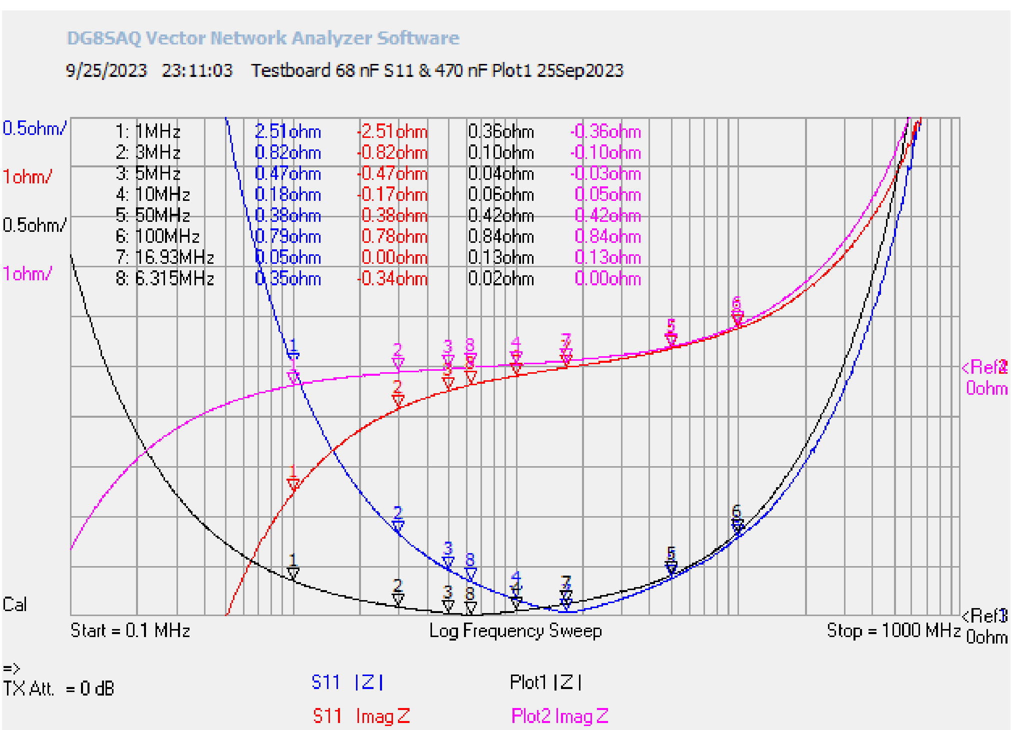
Measurements: Samples of the 0.068 and 0.47 µF capacitors in size 0805 were obtained and measured in a simple shop-built test fixture with a DG8SAQ VNWA vector network analyzer. S-parameter and equivalent impedance measurements and insertion loss were made over the frequency range 100 kHz to 1000 MHz.

The test fixture was made from a PCB with SMA connectors and 0.1 inch pitch socket strips (below-left with a capacitor under test). A plug-in fixture like this has some inherent variability but does provide sufficient accuracy for the comparisons with factory capacitor measurements. The calibration components (Short, Open, Load, Thru) and capacitors were soldered to 2-pin pin strips (below-right).

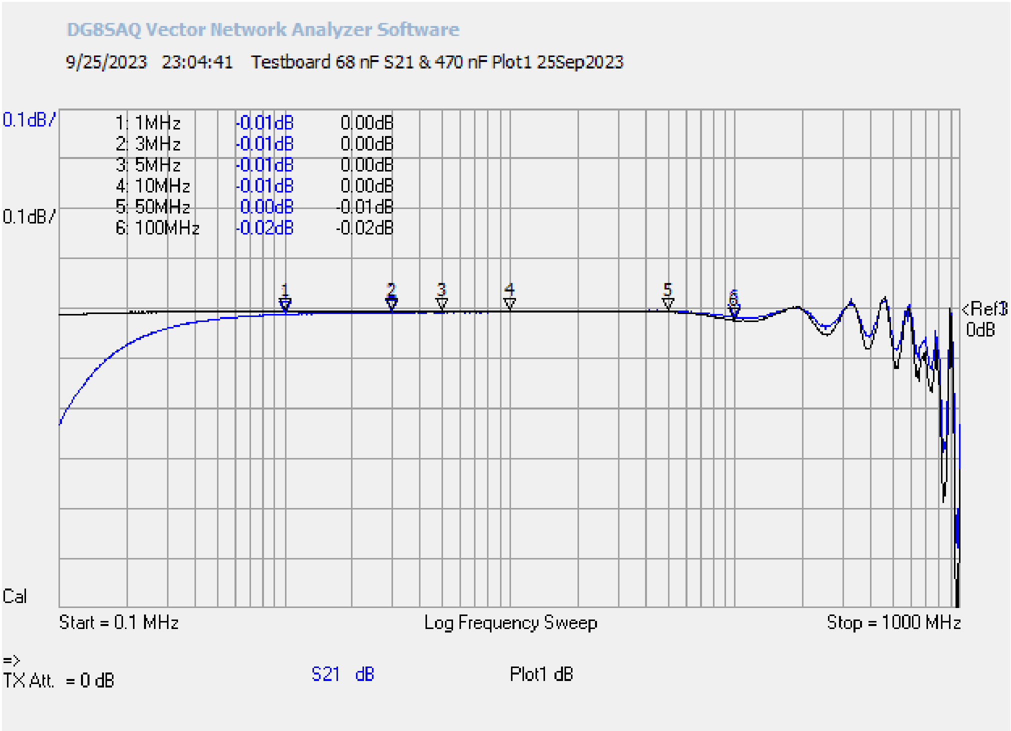




The sockets and pin strips allow easy calibration and the capacitors to be installed in both shunt and series configurations. In the shunt configuration, the primary measurement was S11 reflection coefficient displayed as impedance magnitude |Z| and imaginary impedance ImagZ in ohms. In the series configuration, the primary measurement was S21 transmission coefficient displayed in dB. The plots below show |Z| and ImagZ in the upper plot and S21 in the lower plot.



The blue trace in the is the impedance magnitude |Z| and the red trace is the reactance ImagZ of the 68 nF capacitor and the black and magenta traces are of the 470 nF capacitor.



The blue and black traces are the transmission coefficients (S21) in dB of the 68 nF and 470 nF capacitors, respectively.

The vertical scale *per division* for each trace is shown along the upper-left edge. The frequency range is shown along the bottom horizontal scale as Start and Stop frequencies. Note that the Wurth plots in the previous section use a logarithmic vertical scale whereas the measurements use a linear vertical scale.

The transitions from capacitive to inductive reactance for both capacitors are clearly seen at the center of the dips in |Z| and zero values for ImagZ. The SRF of the 68 nF capacitor is approximately 16.9 MHz (marker 7) and of the 470 nF cap is approximately 6.3 MHz (marker 8), very similar to the Wurth data. The measured reactance of the Wurth 68 nF capacitor at 1 MHz is –j2.51 ohms (red marker 1), equivalent to a capacitance of 63.4 nF, and comparable to –j2.58 ohms from the Wurth data. Similarly, the measured reactance of the Wurth 470 nF capacitor is –j0.36 ohms (magenta marker 1) at 1 MHz, equivalent to a capacitance of 44.2 nF and comparable to –j0.38 ohms from the Wurth data.

References:

- Mini-Circuits, APPLICATION NOTE: Transient Protection of Darlington Gain Block Amplifiers, AN-60-034 Rev. : A M150261 (04/14/15) File: AN60034.DOC
- Wurth Elektronik REDEXPERT website: https://redexpert.we-online.com/we-redexpert/en/#/redexpert-embedded

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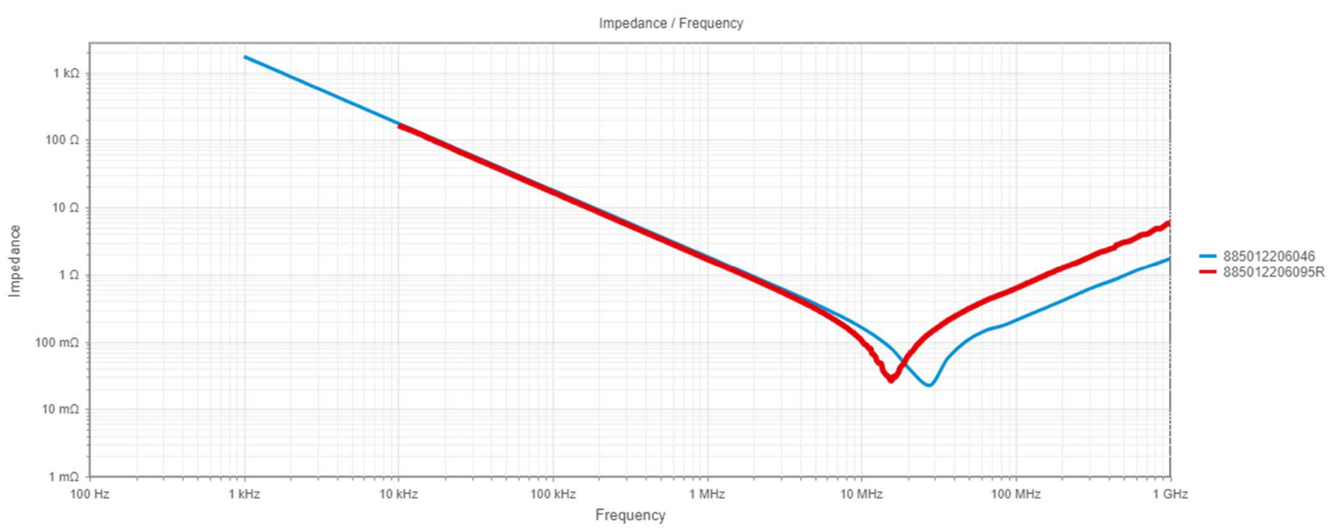
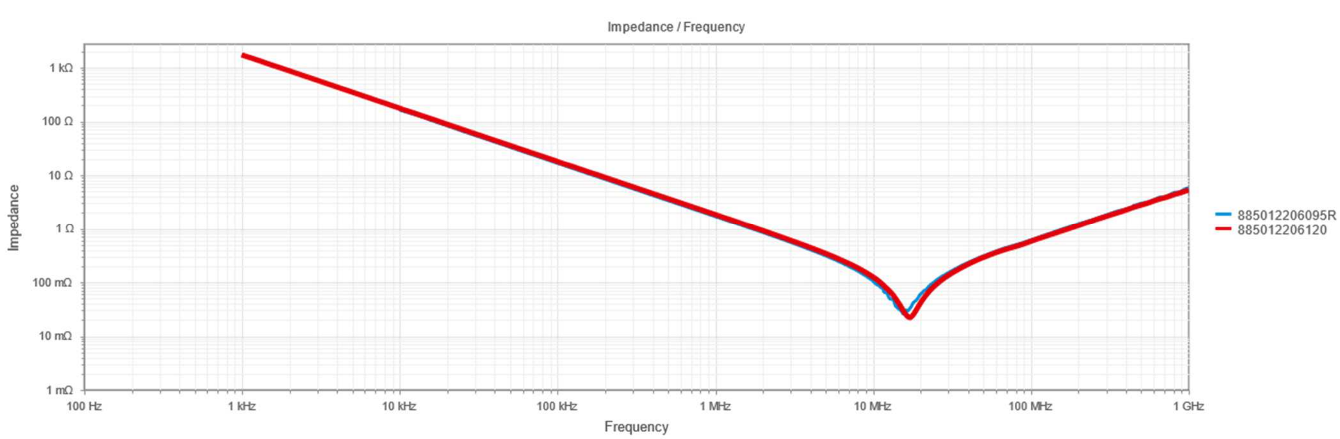
Addendum ~ 17 September 2024:

Increasing the input coupling capacitors from 0.068 to 0.100 µF was considered during Prototype testing to determine if the original capacitors affected the input impedance. Three Wurth capacitors were considered with voltage ratings of 16 V, 50 V and 100 V as follows:
p/n 885012206046: 0.100 µF, 0603, 16 Vdc, X7R, ±10% tolerance
p/n 885012206095R: 0.100 µF, 0603, 50 Vdc, X7R, ±10% tolerance
p/n 885012206120: 0.100 µF, 0603, 100 V, X7R, ±10% tolerance.

Note that all X7R capacitors are subject to capacitance change due to their operating environment – particularly bias voltage and temperature – but this is not considered a factor in their application here.

The plotted impedance of the 16 V 0.100 µF capacitor (blue trace in image directly below) is approximately 0.538 ohms at 3 MHz and 0.195 ohms at 100 MHz. The plotted impedance of the 50 V 0.100 µF capacitor (red trace in image directly below) is approximately 0.538 ohms at 3 MHz and 0.647 ohms at 100 MHz. The plotted impedance of the 100 V 0.100 µF capacitor(red trace in the bottom image) is approximately the same at both frequencies.





All three capacitors meet the requirements previously stated (≤ 1 ohm impedance at high and low frequencies). The 100 V part is recommended for the input circuit because it is exposed to the 15 Vdc FEE voltage and transients from the outside plant; the 100 V rating provides additional margin.

Document Information

Author: Whitham D. Reeve

Revisions: 0.0 (Original draft started, 05 Sep 2023)

0.1 (Added Wurth capacitor data, 07 Sep 2023)

0.2 (Corrected p/n for the Wurth 0.068 μF capacitor, 15 Sep 2023)

0.3 (Added measurements, 25 Sep 2023)

0.4 (Added test fixture images & description, 26 Sep 2023)

0.5 (Distribution, 29 Sep 2023)

0.6 (Added plots and impedances for 0603 Wurth capacitors, 5 Dec 2023)

0.7 (Addendum for 0.100 μF capacitors, 17 Sep 2024)

Word count: 1340

File size (bytes): 3210314

Memo Cover Sheet

ARX-Eval-12

Application of the TI TPS16412 eFuse in the Rev. I ARX

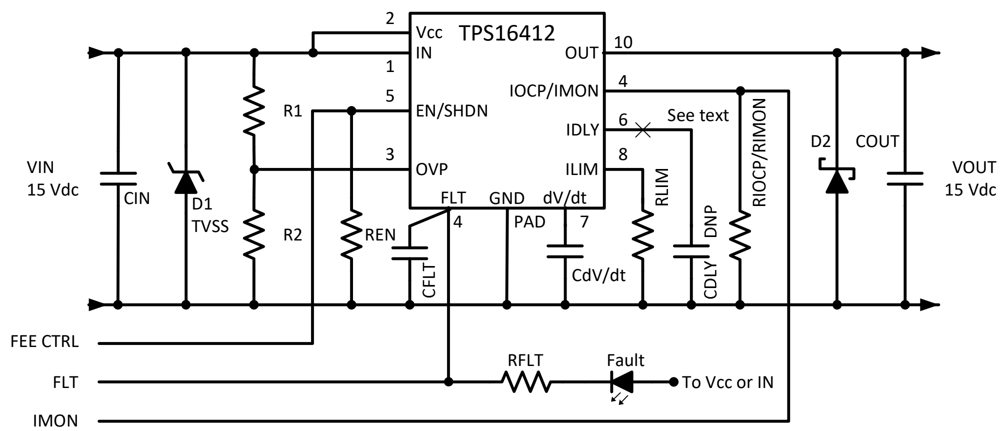
Whitham D. Reeve

12 October 2024

Application of the TI TPS16412 eFuse in the Rev. I ARX (includes Addendums 1 & 2)
Whitham D. Reeve

The TPS16412 is an integrated FET power management device and includes overvoltage protection, inrush control, current limiting, overcurrent protection, short-circuit protection and load current and fault monitoring. The device is supplied in the VSON or very-thin small-outline no-lead package. Device dimensions are 3 x 3 x 1 mm (LxWxH).

In the ARX application, the device provides FEE power feed and on/off switching control, overvoltage protection, current limiting, overcurrent protection and current and fault monitoring. Current limiting and overcurrent protection is used to prevent damage to the ARX and FEE bias-tee inductors from coaxial feedline faults that cause an overcurrent condition. The schematic and component values below (revised by Addendums 1 and 2) show the device configuration in the ARX. The components are described in the following sections along with calculations based on the methods described in the manufacturer's datasheet. A block diagram of the eFuse are shown at the end of this report.



Summary of components:

Component	Value	Remarks	
R1	1 Mohm, 1%	OCP voltage divider	
R2	68.1 kohm, 1%	OCP voltage divider	
REN	4.7 kohm, 1%	Enable pull-down	Addendum 1
CdVdt	0.68 µF, 50 V, 5%		
RLIM	27.4 kohm, 1%		Addendum 2
RIOCP	41.2 kohm, 1%		Addendum 2
RFLT	Depends on LED	LED current limit	
CDLY	Not used (see text)	Connect pin to GND or open	
CFLT	1 nF, 50 V		
D1	18 to 36 V	SMAJ-series	Littelfuse TVS
D2	60 V	B260A or B360A	Diodes, Inc. Schottky
COUT	10 µF + 0.1 µF	Both MLCC, Low ESR	
CIN	1 µF + 0.1 µF	Both MLCC	

Note 1: REN added by Addendum 2
Note 2: RLIM changed by Addendum 3 to increase the current limit to 360 mA
Note 3: RIOCP changed as a result of Addendum 2

The eFuse defines and monitors several currents: INRUSH < IOUT < ILIM ≤ IOCP ≤ IFast-trip ≤ ISCP, where INRUSH is the momentary current through the eFuse when it is turned on and it charges the capacitance on its output, IOUT is the load current, ILIM is the design current limit, IOCP is the design overcurrent protection threshold current that allows momentary overcurrent, IFast-trip is the fault current above the overcurrent protection threshold, and ISCP is the short-circuit protection current. The INRUSH, ILIM and IOCP are configurable. The IFasttrip is internally set to 1.9X IOCP and ISCP is internally set to 6.7 A. The IFast_trip and ISCP invoke delay timers that allow momentary currents such as those from motor starting and capacitor charging.

Enable and shutdown input: The EN/SHDN pin controls the eFuse. Setting this pin high turns on the device. Holding the EN/SHDN pin low for more than tLOW_SHDN (24 ms) puts the eFuse into low power shutdown mode in which internal device components are turned off. According to the datasheet (section 7.5), the thresholds are 1.2 V for the rising condition on the EN/SHDN pin and 0.59 V for the falling condition. The maximum allowed voltage on the EN/SHDN pin is 5.5 V.

Addendum 1 ~ eFuse Enable Pull-Down Resistor

The eFuse datasheet sect. 7.5 says the open circuit Enable voltage (VEN-Open) on pin 5 Enable is 4.9 V. This voltage is produced internally and will enable the eFuse when the pin sees an open circuit.

For each channel-pair, the Enable pin 5 on each eFuse is connected directly to P16 (polarization B) and P17 (polarization A) on the MAX7301 port expander. The MAX7301 powers up with P16 and P17 set as GPIO inputs (Table 4 of MAX7301 datasheet), and the input leakage current IIH and IIL is ±100 nA. This can be considered an open circuit in the context of the eFuse Enable input. Thus, the eFuse is enabled until the associated port expander port is configured as an output and pulled low. This can be fixed by using a pull-down resistor on the eFuse Enable pin 5.

The eFuse Enable pin leakage current IEN is –10 µA minimum, and the enable threshold voltage for a rising input VENR is 1.2 V and for a falling input VENF is 0.59 V. Thus, it is necessary to ensure that the voltage drop across the pull-down resistor is << 0.59 V, say, for example, 0.59 V/10 = 0.06 V.

The combined current through the pull-down resistor is –10 µA ± 0.1 µA = –9 to –10.1 µA. To limit the voltage drop to the example 0.06 V, the pull-down resistor resistance range is (0.06 V)/(–9 to –10.1 µA) = 6 667 to 5 941 ohms. Lower resistance values would provide lower voltages.

For example, a 4.7 kohm pull-down resistor would limit the voltage drop to (–9 to –10.1 µA) x 4.7k = 0.042 to 0.048 V. A 4.7 kohm resistor is chosen for this application.

IN to OUT resistance: According to the datasheet (section 7.5), the resistance RON across the IN and OUT pins when the device is turned on can be as low as 96 mohm at low temperatures to as high as 215 mohm at 85 °C. A typical value is 153 mohm. With 240 mA FEE operating current, the typical voltage drop across the eFuse is 37 mV and the maximum voltage drop is 52 mV.

Overvoltage protection: The overvoltage protection thresholds are adjusted by connecting the OVP pin through a resistive voltage divider R1 and R2 to the input voltage IN pin. The overvoltage protection function may be disabled by connecting the OVP pin to GND.

The eFuse turns off the internal FET and pulls the FLT pin low if the voltage on the OVP pin rises above the threshold voltage VOVPR. If the voltage on the OVP pin subsequently falls below OVPF, the internal FET is turned on and the FLT pin is pulled high through a pull-up resistor.

According to the datasheet (section 9.5), the pull-up resistor should limit the current to 3 mA on the FLT pin. Therefore, for a 15 V supply voltage, the RFLT should be > 5 kohms; the suggested value for the ARX application is at least 10 kohms. The FLT pin may be pulled high through a low-current fault indicating LED and appropriate current limiting/pull-up resistor.

The rising overvoltage protection VOVPR and falling overvoltage protection OVPF thresholds are set according to the datasheet (section 9.2.2.1) by

$$OVPR = VOVPR \cdot \frac{R1+R2}{R2} \text{ ohms} \tag{1}$$

$$OVPF = VOVPF \cdot \frac{R1+R2}{R2} \text{ ohms} \tag{2}$$

Only the rising overvoltage protection function is used in the ARX application. The rising overvoltage protection threshold setpoint OVPR is set below the FEE voltage regulator maximum voltage (26 V continuous and 60 V for 100 ms transients) or eFuse device maximum voltage (40 V), whichever is lower. In this application, OVPR = 24 V to be conservative. According to the datasheet (section 7.5), the OVP pin voltage for the rising condition VOVPR = 1.48 to 1.58 V (minimum, maximum) and for the falling condition OVPF = 1.34 to 1.46 V (minimum, maximum).

Only the rising condition is considered. Solving equation (1) for R2 gives

$$R2 = \frac{VOVPR \cdot R1}{\left(OVPR - VOVPR\right)} \text{ ohms} \tag{3}$$

In this application, R1 is set to 1M ohms. Substituting OVPR (24 V), R1 (1 Mohm) and typical VOVPR (1.53 V) gives

$$R2 = \frac{VOVPR \cdot R1}{\left(OVPR - VOVPR\right)} = \frac{1.53 \cdot 1M}{\left(24 - 1.53\right)} = 68.1 \text{ kohms} \tag{4}$$

The nearest 1% resistor value is 68.1 kohms.

For VOVPR minimum and maximum datasheet values of 1.48 and 1.58 V, the rising overvoltage protection setpoints are

$$OVPR(\min) = VOVPR(\min) \cdot \frac{R1+R2}{R2} = 1.48 \cdot \frac{1M + 68.1k}{68.1k} = 23.2 \text{ V} \tag{5}$$

$$OVPR(\max) = VOVPR(\max) \cdot \frac{R1+R2}{R2} = 1.58 \cdot \frac{1M + 68.1k}{68.1k} = 24.8 \text{ V} \tag{6}$$

Output slew rate and inrush current control (dV/dt): The inrush current through the eFuse when it turns on is directly proportional to the load capacitance COUT and rising voltage slew rate SR. According to the datasheet (section 8.3.3), the slew rate is

$$SR(V/s) = \frac{IINRUSH(A)}{COUT(F)} \text{ V/s} \tag{7}$$

Alternatively,

$$IINRUSH(A) = SR(V/s) \cdot COUT(F) \text{ A} \tag{8}$$

There is an advantage to slowing the voltage slew rate at the v1.8 FEE to reduce damaging transients on the MCL GALI-6+ output stage amplifier during voltage ramp-up. Mini-Circuits recommends 100 ms ramp-up time. For a 100 ms ramp time, the slew rate would be 15 V/100 ms = 150 V/s. The slew rate is configured as described later. Assuming COUT is 10 µF, the inrush current IINRUSH would be

$$IINRUSH(A) = SR(V/s) \cdot COUT(F) = 150 \cdot 10 \cdot 10^{-6} = 1.5 \cdot 10^{-3} \text{ A = 1.5 mA} \tag{9}$$

The average power dissipation PDINRUSH inside the eFuse during inrush may be calculated from

$$PDINRUSH(W) = \frac{IINRUSH(A) \cdot VIN(V)}{2} \text{ W} \tag{10}$$

In the ARX application

$$PDINRUSH(W) = \frac{IINRUSH(A) \cdot VIN(V)}{2} = \frac{1.5 \cdot 10^{-3} \cdot 15}{2} = 0.011 \text{ W} \tag{11}$$

For a given power dissipation, the thermal shutdown time of the eFuse must be greater than the ramp-up time to avoid startup problems. The datasheet (section 7.7, figures 7.14 and 7.15) provides plots of thermal shutdown time vs power dissipation for VIN = 12 V and 24 V. The maximum scale for time to shutdown on both plots is 200 ms and the curves are very steep at power dissipation values below 1 W, thus it cannot be reliably determined from the plots if the shutdown time is greater than the ramp-up time. This operational aspect might be determined from the TPS16412 Evaluation Module, and it may be necessary to reduce the ramp-up time from 100 ms to a lower value. In any case, the eFuse protects itself from over-temperature as discussed later.

A capacitor CdVdt may be connected to the dVdt pin to set the voltage slew rate and control the inrush current when the eFuse is turned on. The fastest slew rate is attained by leaving the dVdt pin open but the fastest slew rate value is not given in the datasheet.

Assuming the 100 ms ramp-up time and associated inrush current are suitable from a thermal standpoint, the following calculations may be made. According to the datasheet (section 8.3.3), the capacitance CdVdt in terms of the dV/dt charging current IdVdt and the dVdt Gain GdVdt is calculated from

$$CdVdt(F) = \frac{IdVdt(A) \cdot GdVdt}{SR(V/s)} \text{ F} \tag{12}$$

The recommended range of CdVdt is 10 nF to 5 µF. The datasheet (section 7.5) provides values for IdVdt and GdVdt. Typical IdVdt = 2 µA and GdVdt = 50 V/V. If the slew rate is 150 V/s, as previously used, then

$$CdVdt(F) = \frac{IdVdt(A) \cdot GdVdt}{SR(V/s)} = \frac{2 \cdot 10^{-6} \cdot 50}{150} = 0.67 \cdot 10^{-6}\text{ F} = 0.67\ \mu\text{F} \tag{13}$$

The nearest 5% standard ceramic capacitor value is 0.68 µF.

Active current limiting: The eFuse responds to overcurrent conditions by actively limiting the current when an overload occurs. The device first provides a blanking time configured by a capacitor on the IDLY pin. During the blanking time, the device can provide a current up to overcurrent protection setpoint IOCP. At the end of the blanking time, the eFuse limits current to the current limit threshold ILIM. The blanking time allows the eFuse to ride through motor starting currents or large filter capacitor charging currents. The blanking time delay and IOCP are discussed in the next section.

The current limit setting for the ARX is based on the current carrying capabilities of the bias-tee inductors in the ARX and FEE. The specified ARX inductor (Coilcraft 1205POC-103) can handle approximately 0.5 A for a 40 °C temperature rise above 85 °C ambient and the FEE inductor (Coilcraft 1008PS-472) can handle approximately 1.4 A for a 40 °C temperature rise above 85 °C ambient. The FEE normal operating current is about 240 mA for V2.0 & V2.1 FEE and about 250 mA for V1.8 FEE.

ILIM is set by connecting a resistor RLIM from the ILIM pin to GND. The current limiting accuracy is given in the datasheet (section 3) as ±6%. According to the datasheet (section 8.3.4), RILIM is calculated from

$$RLIM = \frac{0.984 \cdot 10k}{ILIM(A)}\text{ kohms} \tag{14}$$

The recommended range of RLIM is 5.1 to 348 kohms.

Addendum 2 ~ Current Limit Adjustment

An eFuse current limit of 360 mA (240 mA + 50%) is used, in which case

$$RLIM = \frac{0.984 \cdot 10k}{ILIM(A)} = \frac{0.984 \cdot 10k}{0.360} = 27.3\text{ kohms} \tag{15}$$

The nearest 1% resistor value above 27.3 kohms is 27.4 kohms.

Note: The 2-channel prototype ARX board originally used 32.4 kohms to set the current limit to 300 mA, but this was deemed too close to the nominal load current. As a result of this change, the Overcurrent Protection had to be adjusted upward as described below.

Overcurrent protection and blanking time for transient loads: The overcurrent protection setpoint current IOCP must be higher than the current limit ILIM discussed in the previous section by at least 10% margin (this margin is not specified in the datasheet and was provided by a TI applications engineer on the TI Forum). It is controlled by delay timers. When the load current rises above ILIM due to a momentary or continuous overload, the eFuse provides current up to the overcurrent protection setpoint IOCP for the duration of the configurable tIDLY timer (default 6.5 ms) and then reduces the current to ILIM for a maximum duration of the tLIM_DUR timer (default 2X tIDLY = 13 ms). These timers allow the device to ride through momentary transients. The tIDLY timer is configurable as described below but it is not used in the ARX application.

The overcurrent protection setpoint IOCP is configured by connecting a resistor RICOP from the IOCP/IMON pin to GND. According to the datasheet (section 8.3.6), the resistor value is calculated from

$$RIOCP = \frac{2.25A}{IOCP(A)} \cdot 7.32k \text{ ohms} \tag{16}$$

The recommended range of RIOCP is 6.34 to 80.6 kohms. If IOCP is set to 400 mA (current limit of 360 mA plus 10%), then

$$RIOCP = \frac{2.25A}{IOCP(A)} \cdot 7.32k = \frac{2.25A}{0.400} \cdot 7.32k = 41.2k \text{ ohms} \tag{17}$$

The nearest 1% resistor value is 41.2 kohms.

The blanking time for overload and overcurrent events is configured by connecting a capacitor between the IDLY pin and GND. According to the datasheet (section 8.3.6), the tIDLY, or blanking time IDLY, is

$$IDLY = \frac{6.5ms}{12nF} \cdot CDLY(nF) \text{ ms} \tag{18}$$

The recommended range of CDLY is 0.012 to 10 µF. If the IDLY pin is left open or connected to GND, the eFuse disables the blanking time and goes directly to current limiting. The blanking time is not required in the ARX application, so the IDLY pin should be connected to GND or not connected. If connected to ground, a zero ohm resistor may be used so that it can be replaced with a capacitor if a need for CDLY is found in the future.

<u>Fast trip and short circuit protection</u>: According to the datasheet (section 8.3.7), if the output current reaches the short circuit current ISCP level, an output short circuit is detected, and the eFuse turns off the internal FET after a short circuit protection delay tSCP_dly (280 ms). To prevent false tripping during low level input transients, the eFuse uses a fast-trip comparator to turn off the internal FET if the output current exceeds Ifast-trip (1.9 x IOCP).

<u>Analog load current monitor on the IOCP/IMON pin</u>: The eFuse provides an output load monitor current on the IOCP/IMON pin that is proportional to the internal FET current. The resistor RIOCP placed from the IOCP/IMON pin to GND converts the current to a voltage that may be sensed by the ARX control system. According to the datasheet (section 8.3.8), the output current IOUT is calculated from the value of resistor RIOCP (RIMON), the voltage VIMON across the resistor, the IMON/IOUT gain GIMON and IMON offset current OSIMON from

$$IOUT = \frac{VIMON - (OSIMON \cdot RIMON)}{GIMON \cdot RIMON} \text{ A} \tag{19}$$

Note that RIMON in this equation is the same resistor RIOCP determined in the previous section. The values of the gain GIMON range from 45 to 55 µA/A (50 µA/A typical) and the values of the IMON offset current OSIMON range from –0.8 to +0.8 µA (0.05 µA typical). For the RIMON determined in the previous section (47.5 kohm), the typical offset voltage is 2.4 mV.

Addendum 3 ~ Load Current Monitoring

The gain of the eFuse load current monitor in the Rev. I ARX configuration is nominally 50 µA/A, which with the revised RIMON resistor value is equivalent to approximately 2 V/A compared to 10 V/A for the Rev. H current monitor. The gain is determined by the internal configuration of the eFuse as well as the external resistor RIMON. Thus, for example, for a load current of 250 mA, the output voltage from the eFuse is approximately 0.5 V compared to 2.5 V for the Rev. H current monitor. See the document *Evaluation of the TI TPS16412 eFuse for Use in the Rev. I ARX* for measurements and a plot.

The eFuse load current output has a small offset voltage. The calculated offset voltage from the eFuse is a couple mV, approximately equivalent to the error in the Rev. H shunt resistor. In the Rev. H ARX, the equivalent resistance is 0.099 ohms instead of 0.1 ohms because the Rev. H ARX has a 10 ohm resistor is parallel with the 0.1 ohm load shunt resistor.

<u>IN-to-OUT short circuit detection</u>: According to the datasheet (section 8.3.9), if the eFuse detects a resistance less than RSHORT (30 mohm) across the IN and OUT pins, it pulls the FLT pin low. At startup, the eFuse watches for a short across the IN and OUT pins and, if none exists, continues normal startup. After startup the device watches at regular (unspecified) intervals and if a short is detected, the FLT pin is pulled low after a delay tIN_OUT_Short_Detect (135 ms). After a short is detected, the eFuse is latched off. It may be reset by toggling the EN/SHDN pin or the Vcc supply. The EN/SHDN pin must be kept low for at least tLOW_SHDN (24 ms).

<u>Thermal shutdown and overtemperature protection</u>: The eFuse uses automatic shutdown to protect from high internal junction temperatures. The TPS 16412 eFuse does not latch off during thermal shutdown but apparently waits indefinitely for the temperature to lower. It automatically resets when the temperature decreases below a threshold.

According to the datasheet (section 8.3.10), during current limiting, the internal FET power dissipation is (VIN – VOUT) x IOUT, which will cause the junction temperature to increase. If the device junction temperature reaches TTSD (155 °C), the internal FET is turned off. The eFuse will wait for the temperature to go below TTSD – TTSD-hyst, where TTSD-hyst = 12 °C, and the device restarts after a delay tRETRY (8 x tIDLY where the default tIDLY = 6.5 ms). Note that tIDLY may be increased by connecting capacitor CDLY as discussed above, but this is not used in the ARX application.

<u>Application</u>: The eFuse has a relatively large thermal pad underneath that must be connected to GND. The pad is the primary thermal conductive path from the internal FET junction through the PCB to ambient air, so the GND should have as large an area as possible.

The input decoupling capacitor CIN should be ceramic and greater than 10 nF. Transient protection is needed on the input and output of the eFuse to protect it from overvoltages due to inductive kickback when the device interrupts the current during short circuit or overload conditions or when the board is disconnected and reconnected.

According to the datasheet (section 9.5.1), the transient voltage at the eFuse input is estimated from

$$VSPIKE(ABSOLUTE) = VIN + \left(ILOAD \cdot \sqrt{LIN/CIN}\right) \tag{20}$$

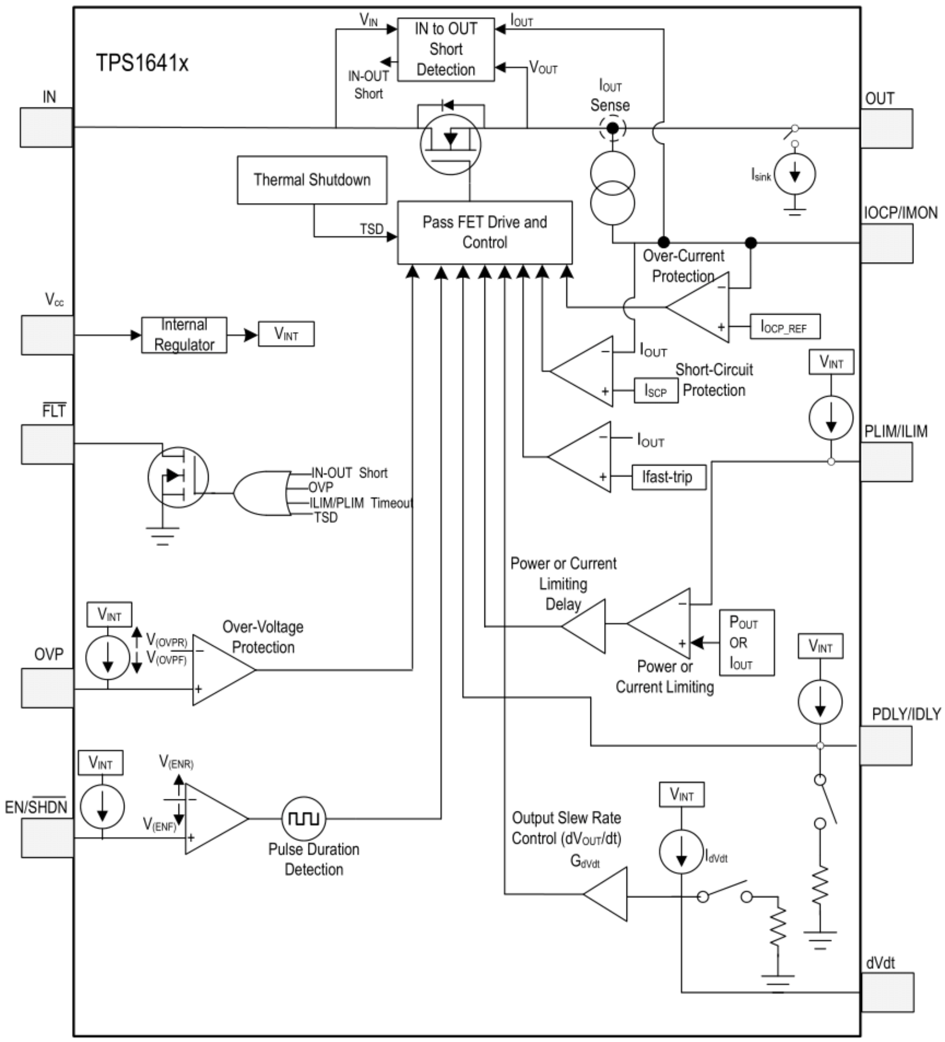
where VIN is the input supply voltage, ILOAD is the load current, LIN is the inductance looking into the source and CIN is the capacitance at the device input. Rather than attempt calculation of the peak spike voltages that might exist in the ARX, a TVSS D1 is placed across the input and a Schottky diode D2 is placed across the output. The eFuse IN pin is rated to 40 V and the Vcc pin is rated to 60 V. The eFuse OUT pin has an absolute maximum voltage rating of –1 V for negative transients.

In the ARX application, the IN and Vcc pins are tied together so a unidirectional TVS diode on the input should be rated no higher than 36 V (40 V – 10%) and no lower than 18.0 V (15 V + 20%). The percentages shown here are not adjusted for TVS diode tolerance. Suitable devices are the Littelfuse SMAJ-series TVS diodes. A Schottky diode is used on the output. A suitable device is rated 60 V such as the Diodes, Inc. B260A (2 A) or B360A (3 A). The protection devices on the input and output should be located as close as possible to the IN and OUT pins they are designed to protect.

The input power supply decoupling capacitor CIN should be placed as close as possible to the IN and GND terminals of the eFuse, and high current carrying power paths must be as short as possible and sized to carry at least twice the full load current (preferably twice the limiting current). The GND terminal must be tied to the PCB ground plane at the eFuse terminal. According to the datasheet (section 9.5.1), the capacitor COUT should be low ESR and larger than 1 µF (previous calculations assumed 10 µF).

The resistors and capacitors used to control the eFuse must be located close to their respective pins with the other ends connected with the shortest possible trace lengths to reduce parasitic effects on the current limit and overvoltage response. The datasheet (Figure 9-11) shows a layout example. Based on comments posted by a TI applications engineer in the TI forum, the FLT pin may be vulnerable to stray coupling to the OVP pin depending on the PCB trace layout so provision should be made for a small capacitor CFLT from the FLT pin to GND to slow down the FLT ramp rate. The recommended capacitor value is 1 nF (this capacitor is not shown in the datasheet but is a known fix for a stray coupling problem on the TPS16412 Evaluation Module).

TPS16412 block diagram:



Document Information

Author: Whitham D. Reeve

Revisions: 0.0 (Original draft started, 07 Apr 2023)
0.1 (1st draft completed 08 Apr 2023)
0.2 (Component summary, 11 Apr 2023)
0.3 (IOCP/ILIM margin added, 12 Apr 2023)
0.4 (Updated current limiting accuracy, 18 Apr 2023)
0.5 (Distribution, 28 Aug 2023)
0.6 (Added Addendum for load current monitoring, 13 Nov 2023)
0.7 (Updated schematic to show pin numbers, 29 Nov 2023)
0.8 (Updated to include Addendums 1 and 2, 24 Aug 2024)
0.9 (Updated Addendum 2, 12 Oct 2024)

Word count: 3624

File size (bytes): 131193

Memo Cover Sheet

ARX-Eval-13

ARX LED Evaluation

Whitham D. Reeve

21 October 2024

ARX LED Evaluations

The table below shows the final LED data to be used in the 16-channel ARX. The forward current, forward voltage and luminous intensity values are from the respective datasheets. Some LEDs are different than in the ARX Prototype. The prototype LEDs and current limiting resistors are shown on the next page.

Function	Color	Mfr	P/N	Vin (V)	If (mA)	Vf (V)	Iv (mcd)	R (ohm)	P (W)	Remarks
Board ID	Yellow	Kingbright	APT3216LSYCK/J3-PRV	3.3	2	1.85	25	725	0.003	
FEE fault	Red	Kingbright	APT3216LSECK/J3-PRV	15.0	1.25	1.8	25	10.56k	0.017	Note 3
15 V bus input	Green	Kingbright	APTD3216LCGCK	15.0	2	1.9	25	6.55k	0.026	Primary V
8.8 V bus input	Green	Kingbright	APTD3216LCGCK	8.8	2	1.9	25	3.45k	0.014	Primary V
3.3 V bus output	Blue	Kingbright	APT3216LVBC/D	3.3	2	2.65	24	325	0.001	Derived V
7.0 V bus output	Blue	Kingbright	APT3216LVBC/D	7.0	2	2.65	24	2.18k	0.009	Derived V
PIC live indicator	?	Kingbright	APT2012LZGCK	3.3	2	2.65	100	649		D34/D35

Table notes:

1 Vin = input voltage to the LED circuit, Vf = *typical* forward voltage of the LED and Iv = *typical* luminous intensity

2. Current limiting resistor R = (Vin – Vf)/If. Theoretical values, not standard values, are shown

3. The rated luminous intensity of the Red LED is 40 mcd at 2 mA. To make it comparable to the other LEDs, If is reduced to rated If x 25/40 = 1.25 mA

Yellow: https://www.kingbrightusa.com/product.asp?catalog_name=LED&product_id=APT3216LSYCK/J3-PRV
Red: https://www.kingbrightusa.com/product.asp?catalog_name=LED&product_id=APT3216LSECK/J3-PRV
Green: https://www.kingbrightusa.com/product.asp?catalog_name=LED&product_id=APTD3216LCGCK
Blue: https://www.kingbrightusa.com/product.asp?catalog_name=LED&product_id=APT3216LVBC/D

The LED information below applies only to the ARX Prototype.

Blue: APT3216LVBC/D, If = 2 mA, Vf = 2.2 V min, 2.65 V typ, 3.0 V max, Iv = 24 mcd typ
D6: 3.3 V output, R = 649 ohm
D14: Port Exp, 3.3 V, R = 649 ohm
D15: Port Exp, 3.3 V, R = 649 ohm
D16: Port Exp, 3.3 V, R = 649 ohm
D17: Port Exp, 3.3 V, R = 649 ohm
D18: Port Exp, 3.3 V, R = 649 ohm
D19: Port Exp, 3.3 V, R = 649 ohm
D20: Port Exp, 3.3 V, R = 649 ohm
D21: Port Exp, 3.3 V, R = 649 ohm
D22: Port Exp, 3.3 V, R = 649 ohm
D23: Port Exp, 3.3 V, R = 649 ohm
D24: Port Exp, 3.3 V, R = 649 ohm
D25: Port Exp, 3.3 V, R = 649 ohm
D26: Port Exp, 3.3 V, R = 649 ohm
D27: Port Exp, 3.3 V, R = 649 ohm
D28: Port Exp, 3.3 V, R = 649 ohm
D36: Port Exp, 3.3 V, R = 649 ohm
D37: Port Exp, 3.3 V, R = 649 ohm
D38: Port Exp, 3.3 V, R = 649 ohm
D39: Port Exp, 3.3 V, R = 649 ohm
D40: Port Exp, 3.3 V, R = 649 ohm
D41: Port Exp Board ID, 3.3 V, R = 649 ohm

Green: APT2012LZGCK, If = 2 mA, Vf = 2.2 V min, 2.65 V typ, 3.0 V max, Iv = **100 mcd typ**
D8: 7.0 V output (too bright), R = 4.3k ohm
D34: PIC ?, 3.3 V, R = 649 ohm
D35: PIC ?, 3.3 V, R = 649 ohm

Green: APT3216LZGCK, If = 2 mA, Vf = 2.2 V min, 2.65 V typ, 3.0 V max, Iv = **100 mcd typ**
D5: 8.8V input (too bright), R = 6.2k ohm

Red: APT3216LSECK/J3-PRV, If = 2 mA, Vf = 1.5 V min, 1.8 V typ, 2.1 V max, Iv = 25 mcd
D7: 15 V input, R = 13k ohm
D11: eFuse fault, Ch. B, 15 V, R = 13k ohm
D29: eFuse fault, Ch. A, 15 V, R = 13k ohm

This document updated 10/21/2024 to include PIC Live Indicator LEDs (D34/D35)