Design and Development of a Prototype ADC for LWA

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Contents

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1 Introduction

In [1] we identified the Analog Devices AD9230 and AD9211 as acceptable candidate A/Ds for LWA. In [2], a baseline A/D sample rate of 196 MSPS was selected, which made these A/Ds a particularly attractive choice. Vendor-developed evaluation boards for these A/Ds were obtained and tested, with results reported in [3] . In fact, these A/Ds are pin-compatible and use identical evaluation boards. Details of the evaluation board design were determined and reported in [4].

We have now created our own version of Analog Devices' design based on the design reported in Memo 116, but now completely implemented from scratch using our own CAD/development tools. This design is suitable for importation into a LWA digitizer (DIG, as defined in [5]) design. We have constructed this design as a prototype board which is completely compatible with the original evaluation board, and able to be tested in exactly the same manner. This report documents the design and evaluation of this board.

The prototype board has components on both the top and bottom sides. Figure 1 shows the top side of the board, and Figure 2 shows the bottom side.

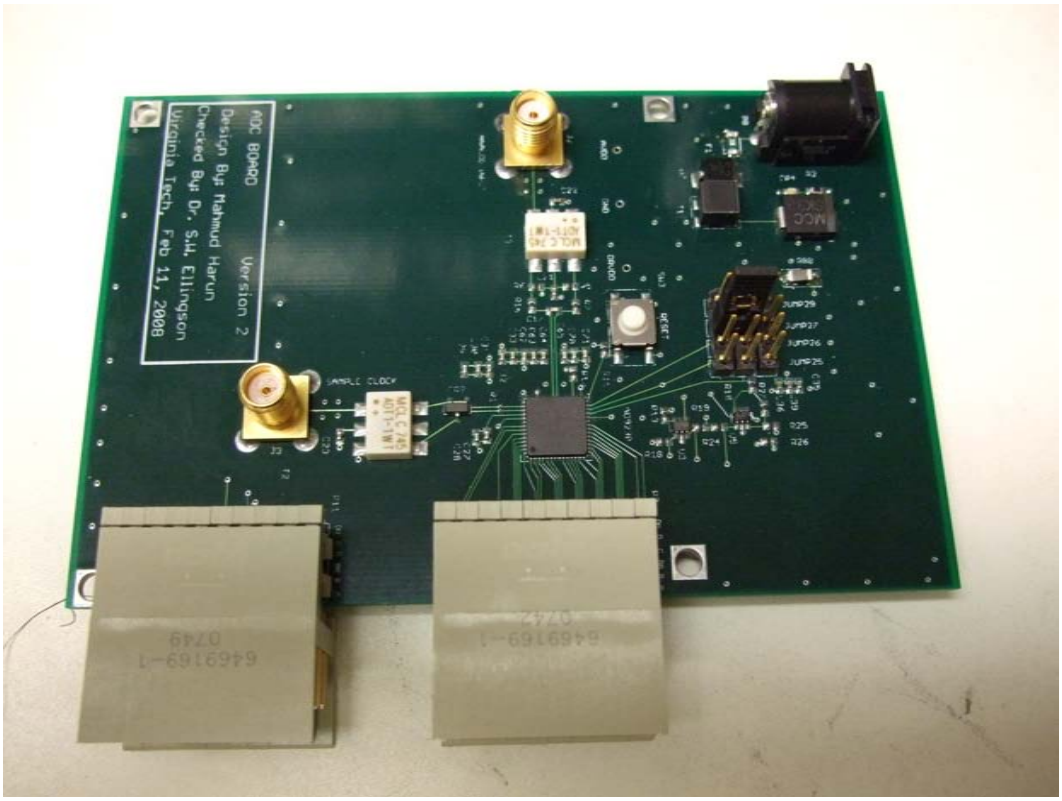

Figure 1: Top side of the VT prototype board.

This report has five sections. The first part lists some key features of the board. The second part provides the full schematic of the board , and the third part shows the layout of the PCB. The fourth section lists the bill of materials and the total cost associated with

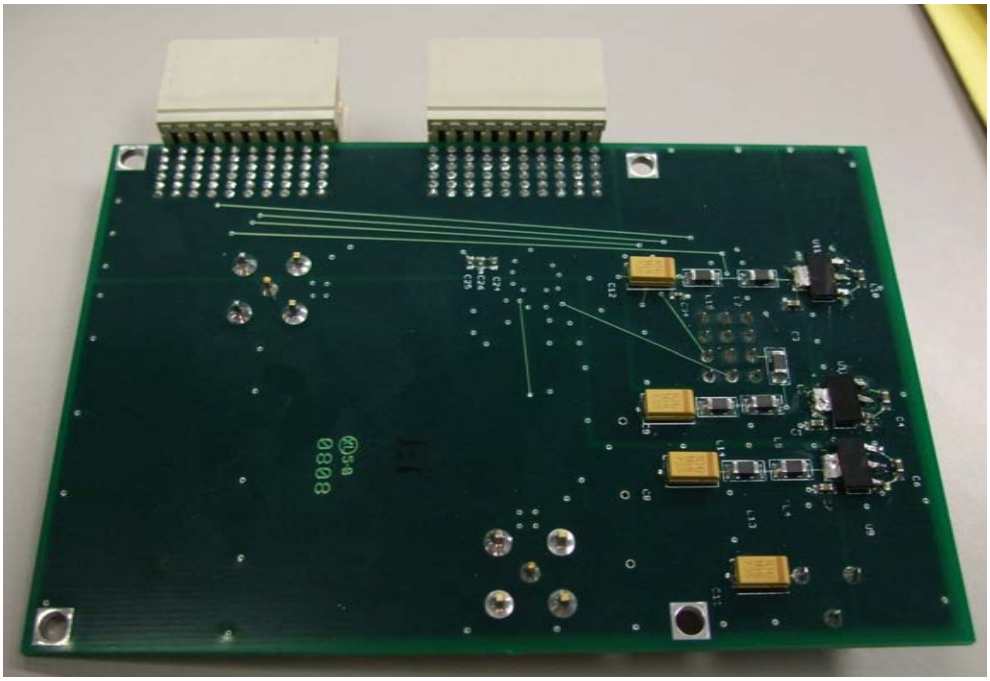

Figure 2: Bottom side of the VT prototype board.

the development of one board. And the last section includes a simple test and the result as an evidence of the board working.

2 Features

2.1 Interface

The prototype board uses the exact same interface as the AD9230-250 evaluation board. As a result it can connect to the HSC-ADC-EVALC board (shown in Figure 3) offered by the vendor. The HSC-ADC-EVALC board is used to buffer high-speed output from the evaluation board which is subsequently transferred to PC via USB.

2.2 Dimension

The dimension of the prototype evaluation board is 10.6 cm $\times$ 6.95 cm. On the other hand, the dimension of the AD9230-250 evaluation board was 13.8 cm $\times$ 11.5 cm. Figure 4 illustrates the comparison in dimension between the prototype board and the original AD9230-250 evaluation board.

In order to incorporate the design of the prototype board into a larger design the "irreducible" dimension of the board needs to be identified. This is the the contiguous area of the board actually occupied by components. As can be seen from Figure 1 there are reducible areas of rectangular shape on the top right and bottom left corners. The dimension of those areas are 3.5 cm $\times$ 1.7 cm and 5.0 cm $\times$ 4.0 cm respectively.

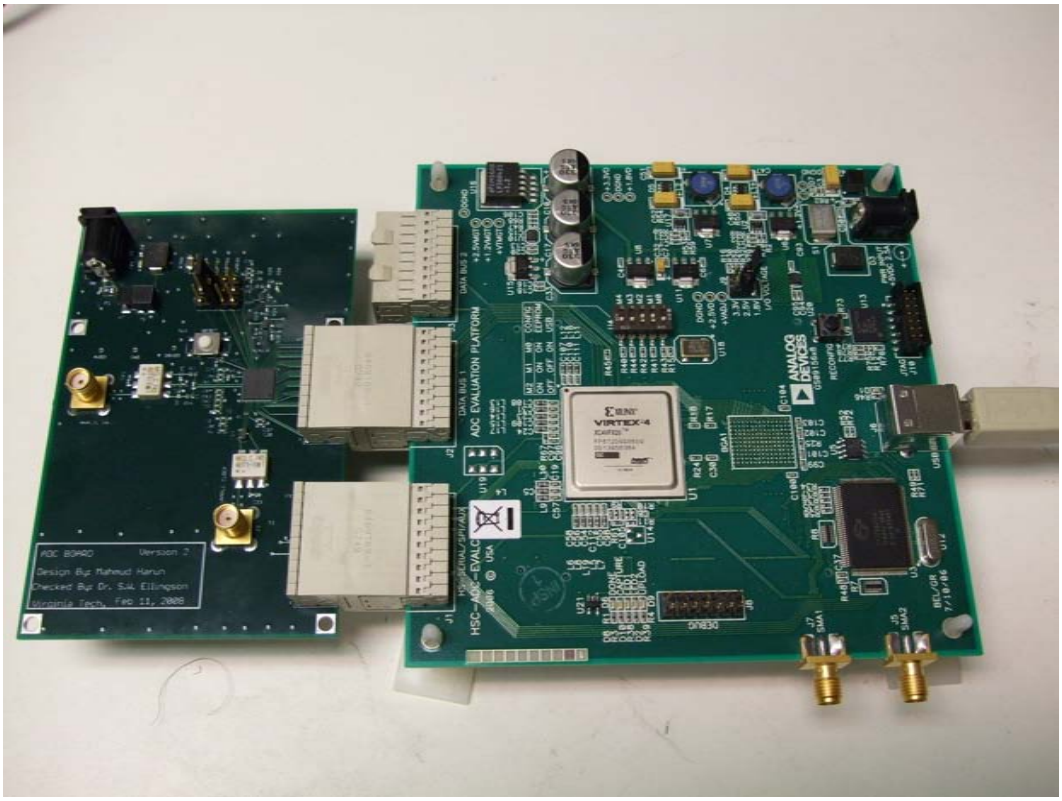

Figure 3: The VT prototype board connected to the Analog Devices HSC-ADC-EVALC board for evaluation.

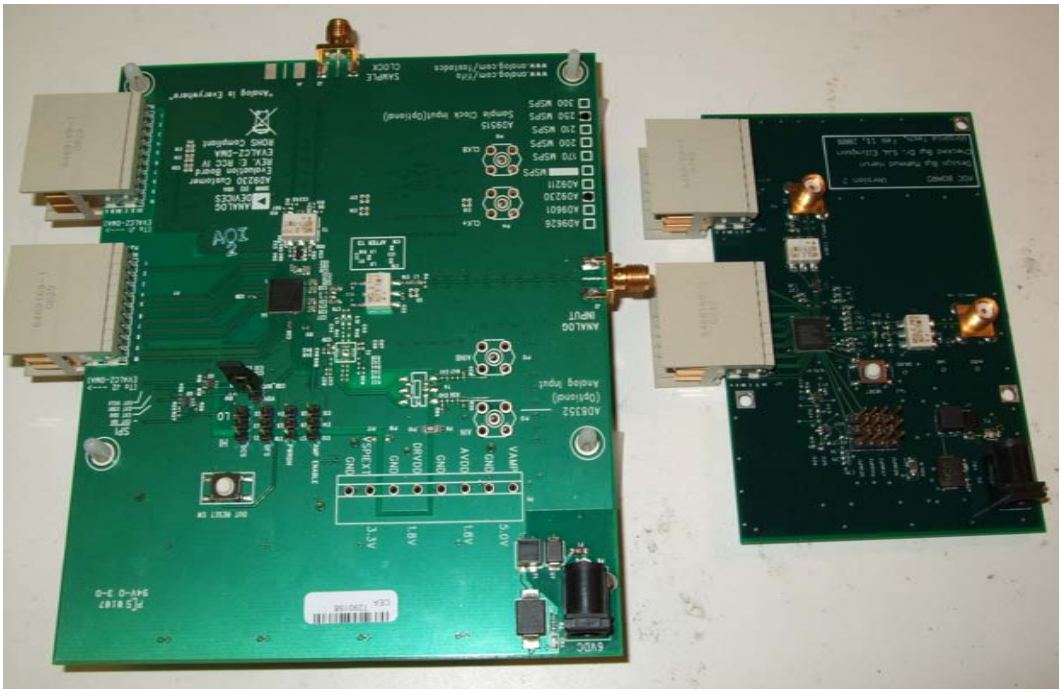

Figure 4: Illustrating the comparison in dimension between the VT prototype board and the AD9230-250 evaluation board.

2.3 Power Consumption

The power consumed by the prototype board is 120 mW; specifically 20 mA at 6 VDC. (These numbers are unchanged from the Analog Devices AD9230-250 evaluation board design.)

3 Schematic

The schematic of the board is divided into three parts. 1) The ADC circuitry (shown in Figure 5)– this part shows the schematic of the analog input, the clock input and the ADC. 2)The Power Distribution circuitry (shown in Figure 6)– this part demonstrates the distribution of power from the power jack (P8 in the schematic). 3)The SPI circuitry (shown in Figure 7)– this part illustrates the circuitry for the SPI interfacing.

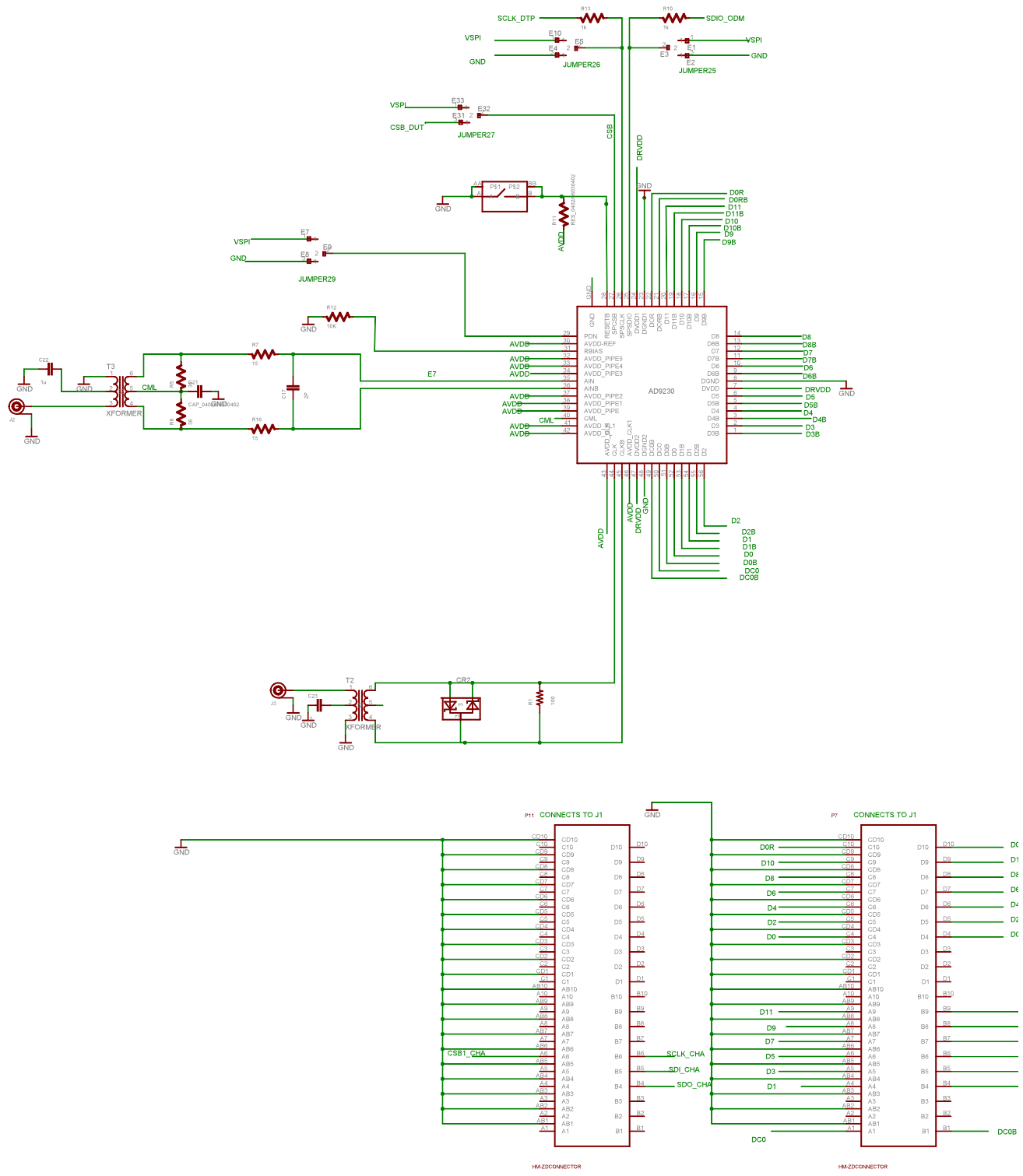

Figure 5: ADC circuitry. [Note. The resistors, capacitors, and inductors are reported in units of ohms, farads and henries respectively.]

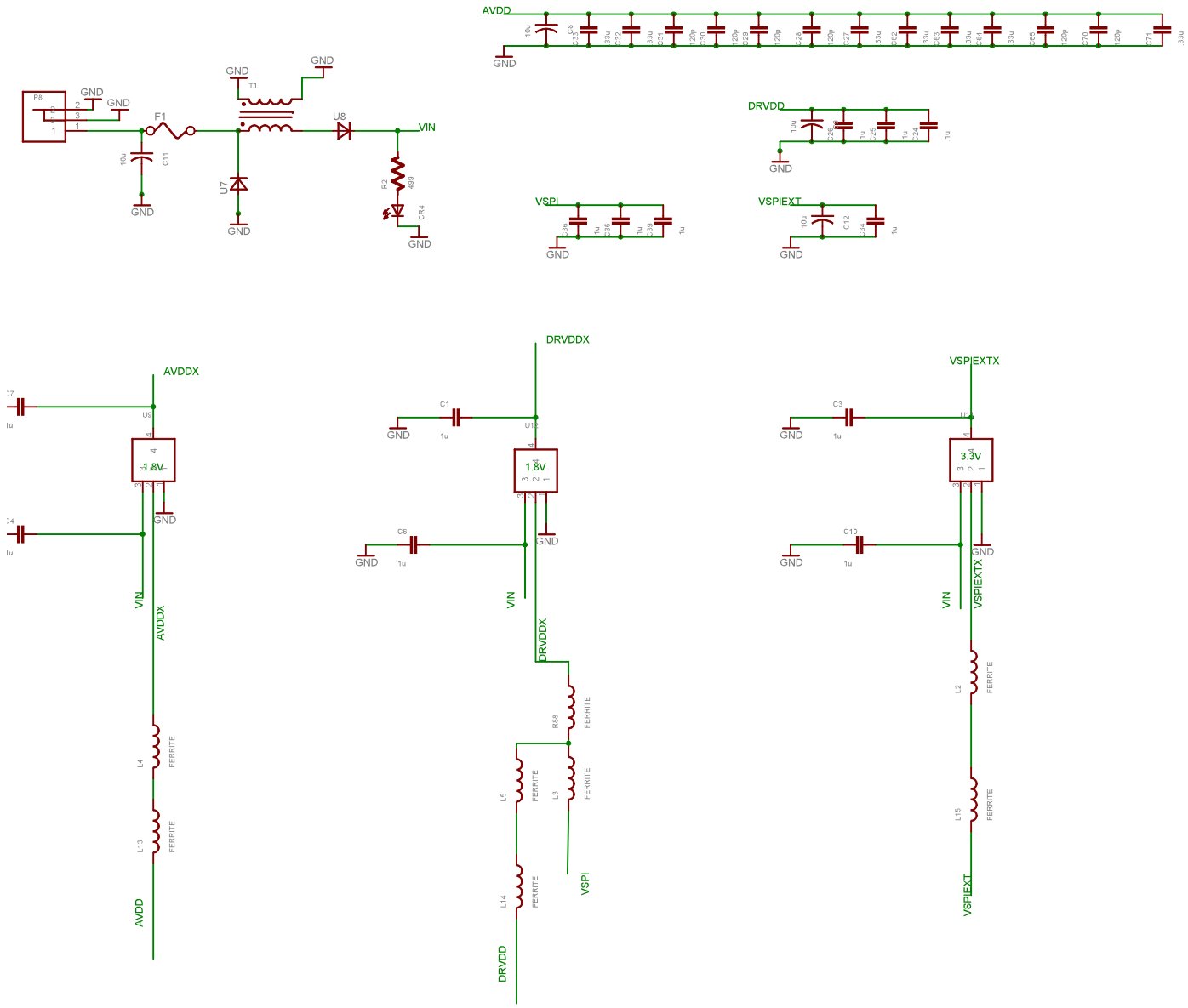

Figure 6: Power Distribution circuitry. [Note. The resistors, capacitors, and inductors are reported in units of ohms, farads and henries respectively.]

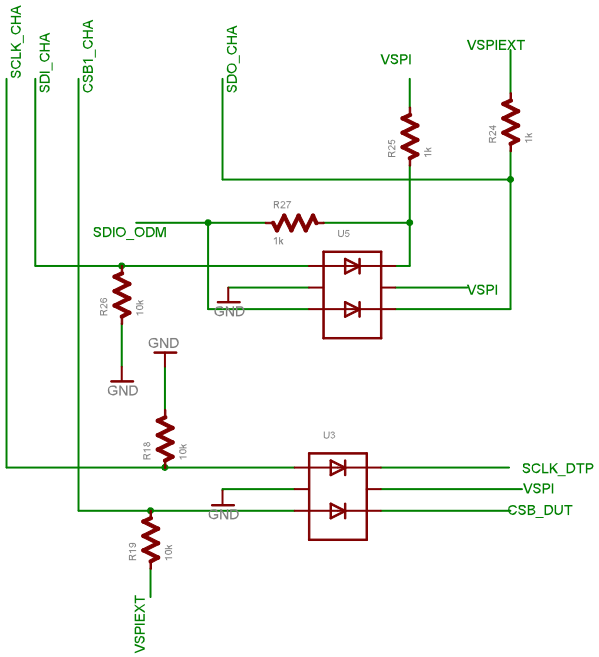

Figure 7: SPI circuitry. [Note. The resistors, capacitors, and inductors are reported in units of ohms, farads and henries respectively.]

4 PCB Layout

This section presents the layout of the board. The board has four layers. The top layer is the primary component side and the bottom layer is the secondary component side. The first inner layer is the ground layer, and the second inner layer is the power layer. The following figures show the layout.

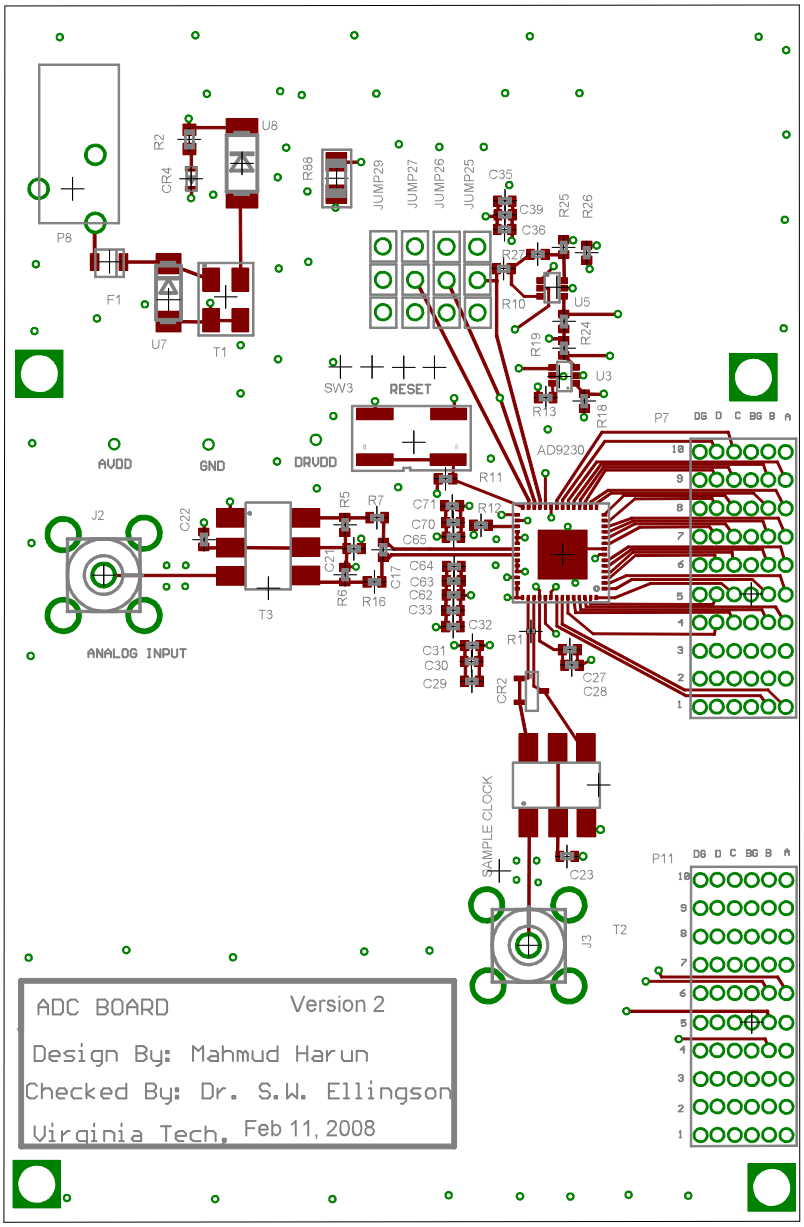

Figure 8: Top Layer

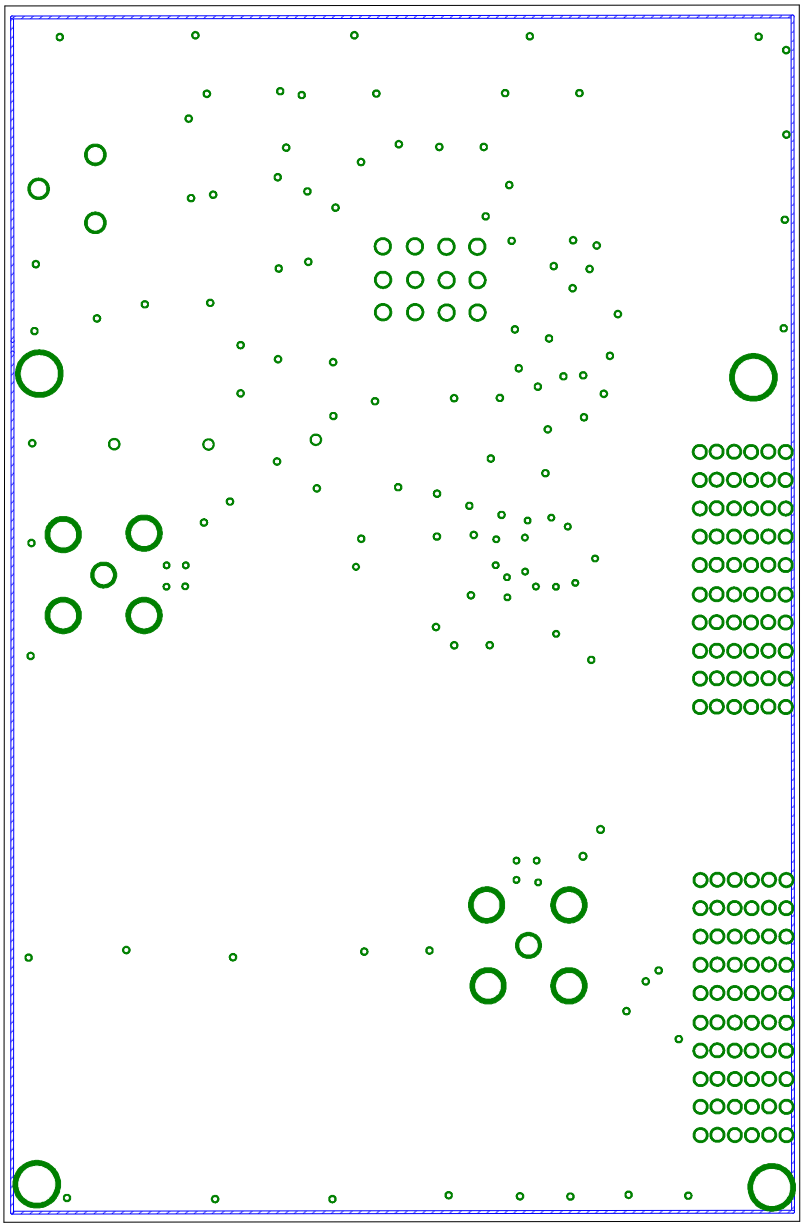

Figure 9: Ground Layer

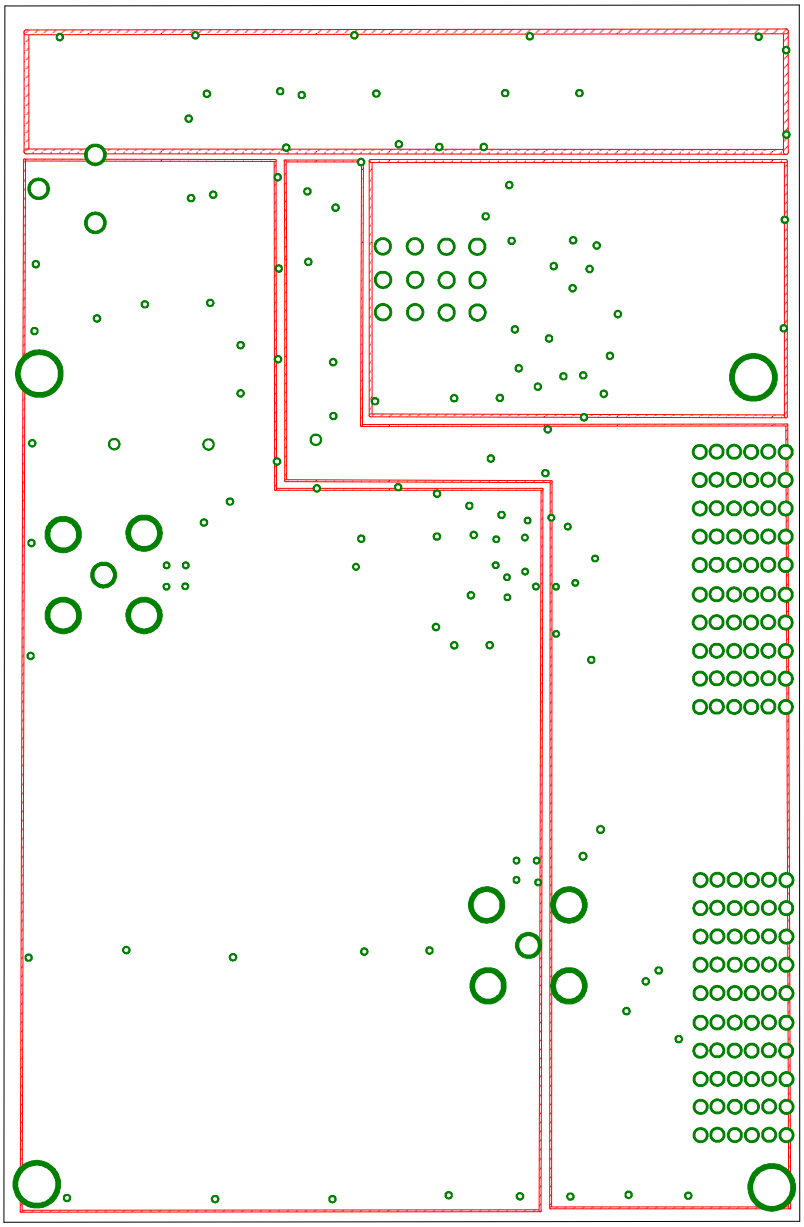

Figure 10: Power Layer

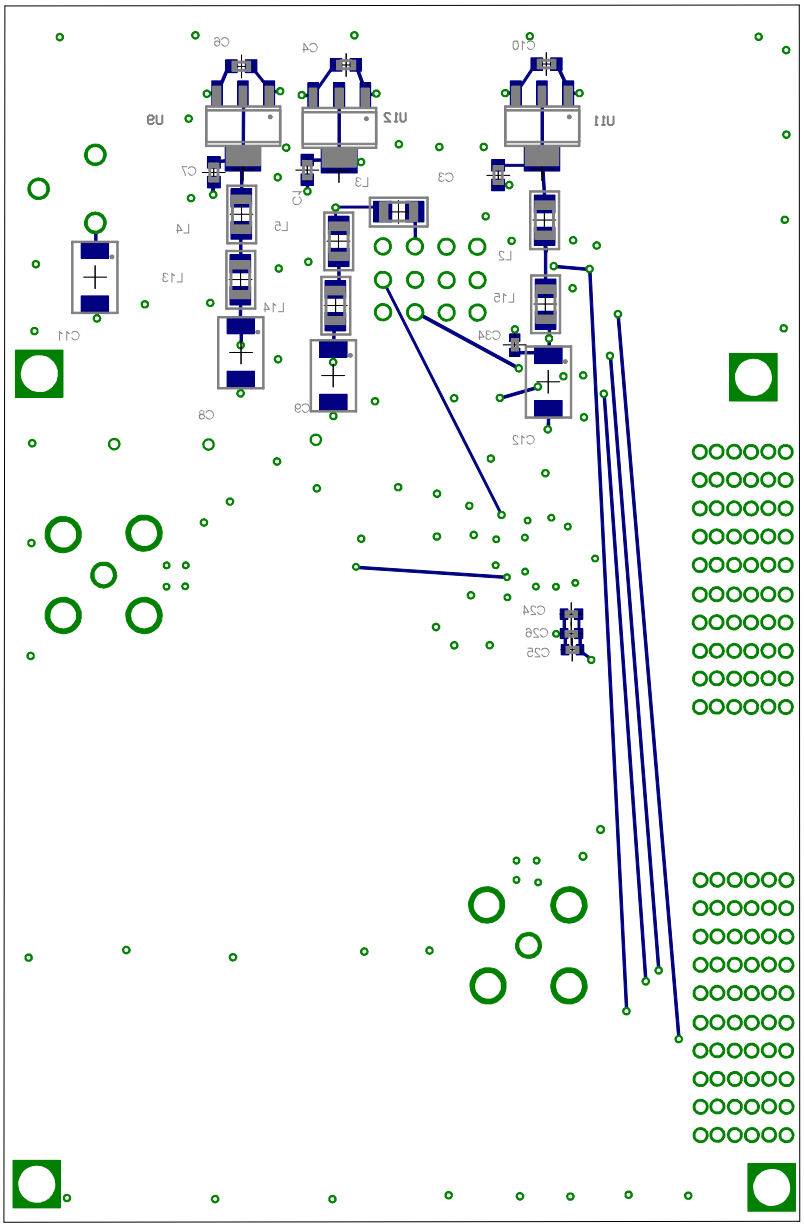

Figure 11: Bottom Layer

5 Bill of Materials and Cost

The bill of materials for the board is shown in Figure 12.

#	QTY	REFDES	PACKAGE	DESCRIPTION	VENDOR	PART NUMBER
2	8	C1,C3,C4,C6,C7,C10	603	CAPACITOR, 1 µF, 0603, X5R, CERAMIC, 6.3V, 10%	Digikey	PCC1915CT-ND
3	6	C8,C9,C11,C12,	6032-28	Capacitor, 10 µF, Tantalum, 16 V, 10% tol	Digikey	399-3732-1-ND
4	1	C17	402	CAPACITOR, 2.0pF 50V CERAMIC 0402 SMD	Digikey	490-3090-1-ND
5	7	C27,C32,C33,C62,C63,C64,C71	402	Capacitor, 0.33 µF, Ceramic, X7R, 25 V, 10%	Digikey	490-3263-1-ND
6	6	C28,C29,C30,C31,C65,C70	402	Capacitor, 120 pF, Ceramic, C0G, 25 V, 5%	Digikey	490-1292-1-ND
7	10	C21,C22,C23,C24,C25.C26,C34,C35,C36,C39	402	Capacitor, 0.1 µF, Ceramic, X5R, 10 V, 10%	Digikey	490-3261-1-ND
8	1	CR4	603	LED GREEN, SMT, 0603, SS-TYPE	Digikey	P11465CT-ND
9	1	CR2	Mini 3P	Diode, 30 V, 20 mA	Digikey	HSMS-2812-TR1G
10	1	F1	1210	Fuse, 6.0 V, 2.2 A trip current resettable fuse	Digikey	NANOSMDC110FCT
11	15	Jump29,Jump27,Jump26,Jump25		CONNECTOR, HEADER 0.1"	Digikey	A26544-ND
12	2	J2,J3,	SMA	Connector, SMA PCB Coax End Launch, Johnson142	Digikey	J494-ND
13	9	L2,L3,L4,L5,L13,L14,L15,R89	1206	Ferrite Bead, BLM, 3A, 50Ω @ 100MHz	Digikey	490-1055-1-ND
14	1	P8		Power Jack, Male, 2.1mm power jack DC	Digikey	CP-102A-ND
15	1	R1	201	Resistor, 100 Ω, 0201, 1/20 W, 1%	Digikey	P100AGCT-ND
16	1	R2	603	Resistor, 499 Ω, 0603, 1/10 W, 1%	Digikey	P499HCT-ND
17	2	R5,R6	402	Resistor, 36 Ω, 0402, 1/16 W, 1%	Digikey	P36JCT-ND
18	2	R7,R16	402	Resistor, 15 Ω, 0402, 1/16 W, 5%	Digikey	P15JCT-ND
19	6	R10,R11,R13,R24,R25,R27	402	Resistor, 1 kΩ, 0402, 1/16 W, 1%	Digikey	P1.00KLCT-ND
20	4	R12,R18,R19,R26,	402	Resistor, 10 kΩ, 0402, 1/16 W, 5%	Digikey	P10KJCT-ND
24	1	SW3	EVQ-Q2F03W	Switch, Light Touch SMD	Digikey	P12937SCT-ND
25	1	T1	2020	Ferrite Bead, 5A, 50V, 190Ω @ 100MHz	Mouser	DLW5BSN191SQ2L
26	2	T2,T3,	CD542	Transformer, 0.5W, 30mA	Mini-Circuits	ADT1-1WT+
27	1	U3	6-SC70	IC, BUFFER, INVERTER, UHS DUAL SC70-6	Digikey	NC7WZ16P6XCT-ND
28	1	U5	6-SC70	IC, BUFFER, INVERTER, UHS DUAL OD OUT SC70-6	Digikey	NC7WZ07P6XCT-ND
29	1	U7	DO-214AA	Diode, 50 V, 2A	Digikey	S2A-TPMSCT-ND
30	1	U8	DO-214AB	Diode, 30 V, 3A, (SMC)	Digikey	SK33-TPMSCT-ND
31	1	U11	SOT-223	Voltage Regulator, 3.3V, 1.5A	Digikey	ADP3339AKCZ-3.3
32	2	U9,U12,	SOT-223	Voltage Regulator, 1.8V, 1.5A	Digikey	ADP3339AKCZ-1.8
33	1	U4	LFCSP	AD9230 12-Bit, 170 MSPS/210 MSPS/250 MSPS, 1.8 V A/D Converter, LFCSP 56P	Analog Devices	R7CT-ND
34	2	P7,P11	HM-Zd PCB	CONNECTOR, 2-Pr 10 Clmn High Speed HM-Zd PCB Mt	Mouser	6469169-1

Figure 12: Bill of Materials

The cost associated with the production of one board is shown in Table 1.

Component	**Cost**	**quantity**
AD9230-250[a]	$97.25	1
Remaining Components other than high-speed digital connectors	$132.52	in small quantities
SUBTOTAL (cost to implement this design on an existing board)	$229.77	1
High speed digital connectors(P7,P11 in the schematic)	$88.24	2
Printed circuit board generation by external vendor[b]	$400.00	1
Board assembly by external contractor[c]	$308.50	1
TOTAL(cost to develop this prototype board)	$1026.51	-

[a]We used the AD9230-250 as it was available to us. We could also use AD9230-210 which has a unit price of $69.23.

[b]IES,Inc.(www.iesgray.com)

[c]IES,Inc.(www.iesgray.com)

Table 1: Cost associated with the development of one VT prototype board.

6 A simple test to check functionality

In this section the results of a simple test performed to check the functionality of the prototype board is presented. A single tone at 5 MHz was applied to the board. The sampling

frequency was 196 MSPS. The time domain plot of a few periods of this signal is shown in Figure 13. Although we have not yet done a full evaluation of the prototype board along the lines of [3], we have compared the single-tone performance to that of the Analog Devices evaluation board, and found that the results appear to be the same.

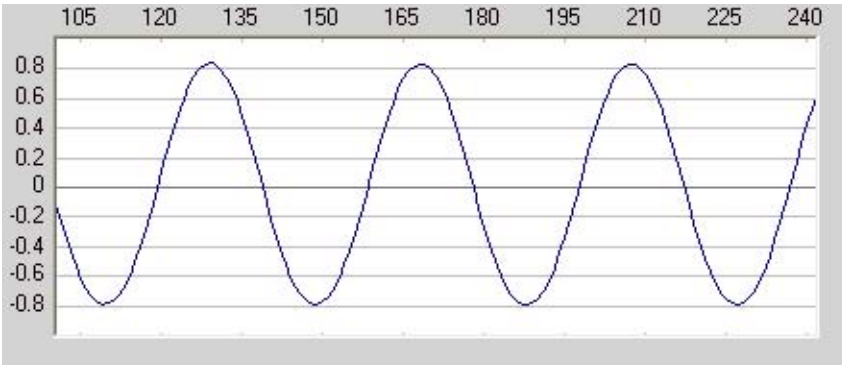

Figure 13: Time domain plot of few periods of a single tone at 5 MHz

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