BFU & DP1 Preliminary Design
Ver. 0.1

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Contents

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1 Introduction

This document presents a preliminary design for the LWA beamforming unit (BFU) level-2 subsystem. Some aspects of how BFUs can be packaged to form the DP1 (level-1) subsystem, which also includes digitizers (DIG), are also addressed. Context for this work can be found in the System Architecture document [1], currently in Version 0.6, which defines the BFU and DP1. The BFU accepts the "full RF" (78 MHz) output from 512 DIGs; where each output represents one polarization from one stand in the station array. The DIG subsystem is described in [2] and the associated "DP1 daisy chain" 4-lane LVDS interface is described in [3]. The BFU performs "delay and sum" beamforming as described in [4]. After delay but before summing, each signal is converted from raw linear polarization to calibrated circular polarization, as described in [5].

The DP1 design shown here, containing all necessary DIGs and 3 complete BFUs, appears to be implementable in the volume of a single standard 19-in rack. It is shown that a single BFU can be implemented using 128 $50 FPGAs. The total cost of a single BFU is estimated to be in the range $20,000–$33,000.

2 Design Concept

In this section the proposed signal flow for the BFU is described. We begin with delay and polarization processing. Figure 1 shows a "Delay and Polarization Module" (DPM), which accepts the signals associated with both raw linear polarizations from a single stand, delays them for beamforming (per [4]), and converts them to calibrated circular polarizations (per [5]). Signals at the input and output to this module are formatted as 12-bit "I" + 12-bit "Q" at 98 MSPS. Each delay FIR is 41 taps with 8-bit real coefficients, which achieves 1.4° maximum phase error over sky frequencies 10–88 MHz as demonstrated in [4]. The preceding FIFO implements a variable delay in the range 0 to 34 samples, again per [4].

Polarization conversion is implemented as a single 2×2 matrix multiply with 8-bit + 8-bit complex coefficients. As explained in [5], this allows perfect (to the limits of coefficient quantization) circular polarization at one frequency, assuming the proper coefficients are known. It is currently unknown whether this is sufficient to achieve acceptable polarization over the entire bandwidth of interest. If greater control over polarization frequency response is required, additional degrees of freedom are available by manipulating the delay FIR coefficients, or the polarization conversion can be expanded into a FIR filter architecture as described in [5]. In the latter case, additional resources could be obtained if needed in a tradeoff by shortening the delay FIRs.

A single FPGA processes two stands simultaneously, as shown in Figure 2. Input signals are resynchronized, echoed transparently to outputs in order to continue the DP1 daisy chain [1], and then deformatted for input to a DPM. Separately, the FPGA accepts a "partial beam" signal in dual circular polarizations, to which the DPM outputs are added. The sum is reformatted and output, becoming the partial beam input for the next FPGA in line. The partial beam inputs and outputs use the DP1 daisy chain format/protocol.

In this scheme, 128 FPGAs are required. They are essentially daisy-chained in serial fashion, with the partial beam result from the last FPGA in the chain being the desired beam, which is sent to the DP2 level-1 subsystem.

3 FPGA Implementation

To confirm the efficacy of the scheme proposed in the previous section, a candidate FPGA was selected and firmware was developed for it. The selected FPGA is the Altera EP3C25, which is one of the "Cyclone III" family of devices [6]. The characteristics of the specific part selected are

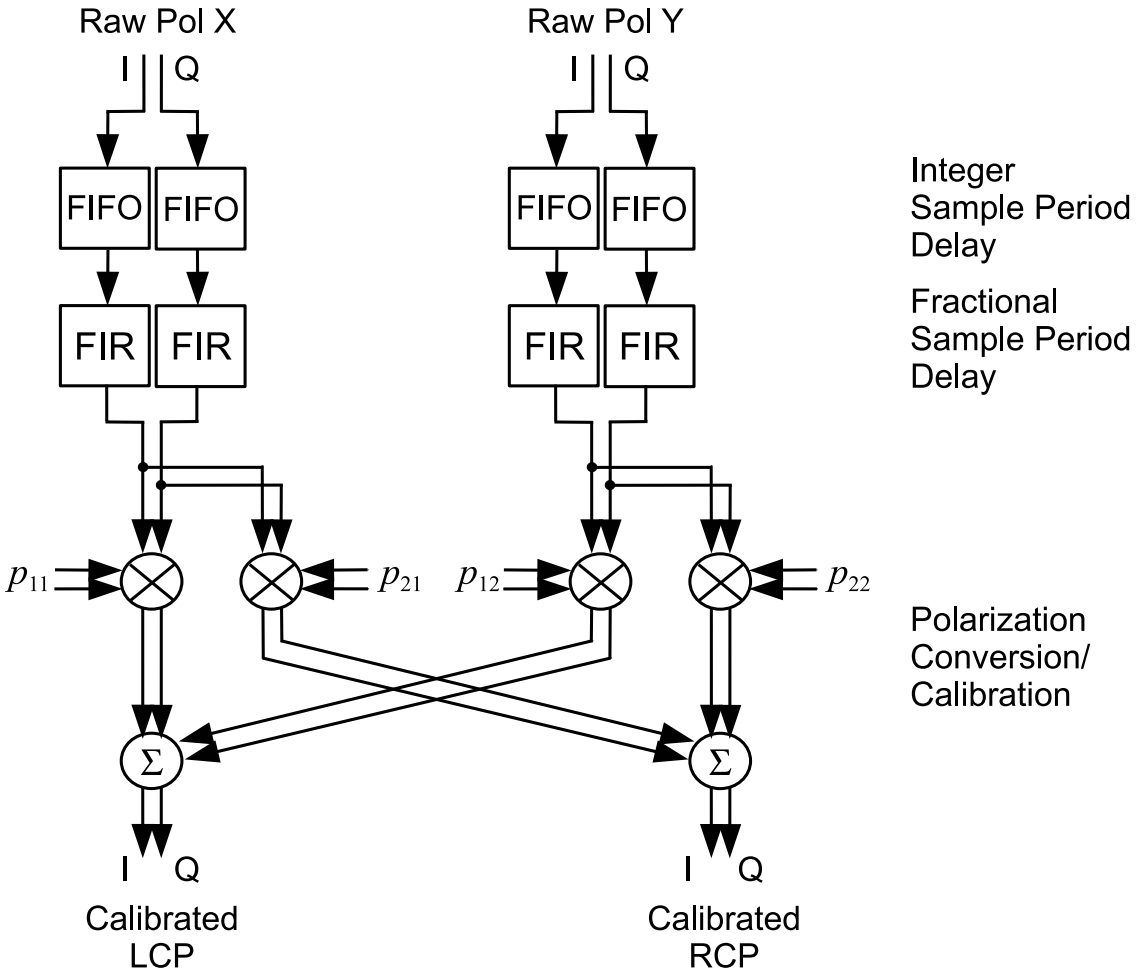

Figure 1: Delay and Polarization Module (DPM). The clock rate is 98 MSPS (equal to the sample rate.) In the scheme described in this document, the FIFOs are all of length 34 samples and the FIR filters are each 41 taps with 8-bit real coefficients. "LCP" and "RCP" refer to left and right circular polarization, respectively.

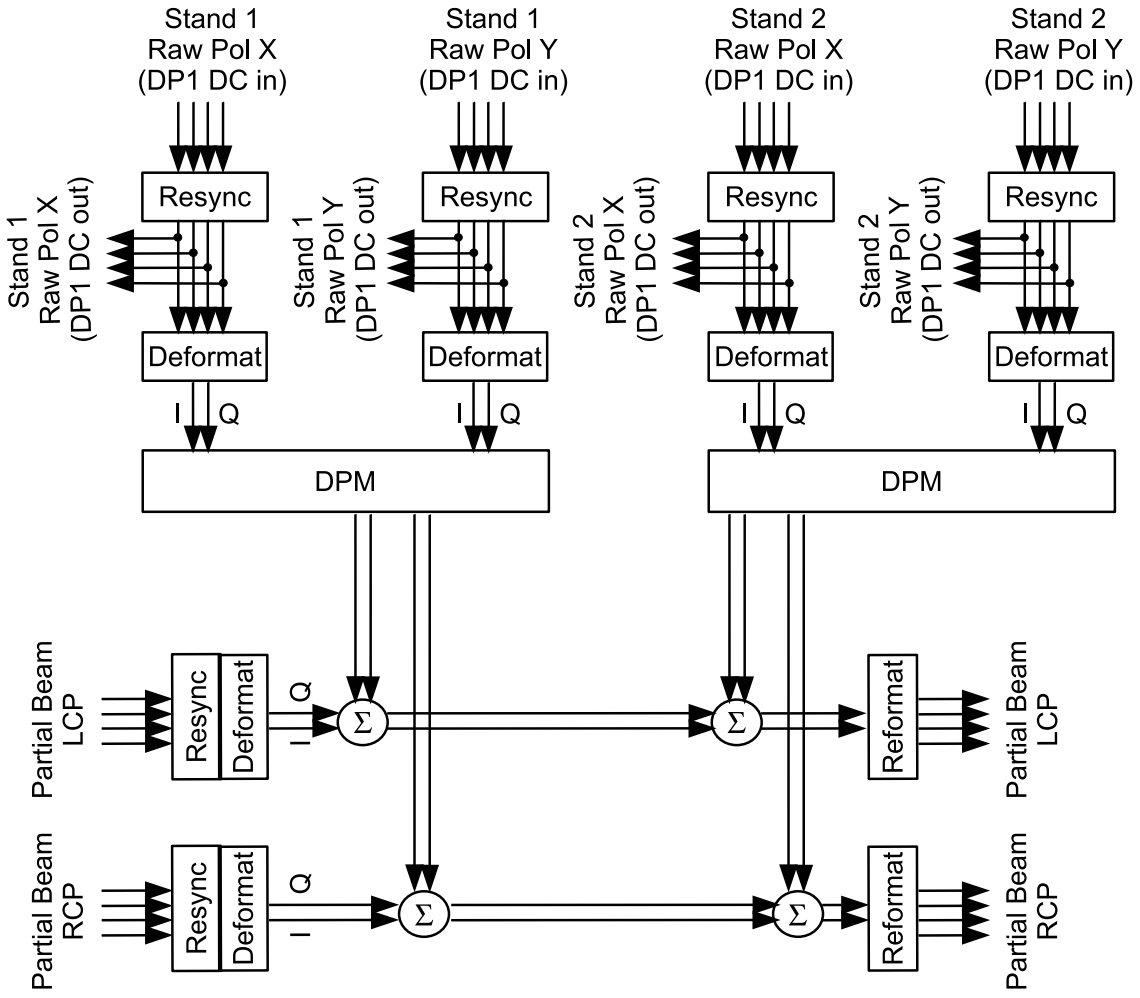

Figure 2: Signal Flow for a single FPGA. The DPMs are elaborated in Figure 1. "DP1 DC" refers to the DP1 daisy chain.

Vendor	Altera
Part Number	EP3C25F324C8 Short form: "EP3C25"
Device Family	Cyclone III
Logic Elements	24,624
Memory	594 Kb
Multipliers	66, each 18×18 bit
PLLs	4
User I/O Pins	216
Differential Channels	71
Package	324-pin FBGA
Price	US$49.30, quantity=1, via Altera on-line store (www.altera.com)

Table 1: Characteristics of the FPGA selected for the preliminary implementation.

summarized in Table 1. Note that this part provides 71 LVDS channels whereas only 48 are required for signal paths (see Figure 2); this leaves ample channels available for clocks and other high-speed signals.

Firmware was developed in Verilog HDL using Altera's Quartus II software, Ver. 7.2. Differences from the scheme shown in Figure 2, implemented in order to reduce design time, are as follows:

- "Resync," "deformat," and "reformat" blocks were not implemented and LVDS pins were not utilized. Instead, all inputs and outputs were routed directly and automatically to available (single-ended) pins, which are available in sufficient quantity. This is not expected to impact conclusions here since ample LVDS channels are available and the logic required to implement the omitted functions is quite lean.
- The DPM delay FIFOs were not implemented. As the capacity of each FIFO is on the order of 34 samples $\times$ 24 bits/sample = just 816 bits, and the associated logic is relatively lean, this is not expected to affect the conclusions.

A summary of the completed design flow is shown in Figure 3. Note that the design consumes 82% of the logic elements on the part, allowing some flexibility in adding additional features. This design achieves timing closure for input clock rates up to 157 MHz; thus the desired 98 MHz is a comfortable fit.

4 Electromechanical Implementation and Cost

In this preliminary design, each FPGA handles two stands; thus, 128 FPGAs are required. At approximately $50 each in small quantities, 128 FPGAs costs $6400. The size of the EP3C25F324C8 FPGA is slightly less than 20 mm $\times$ 20 mm = 400 mm^2. It is a ball grid array package, and thus there is no additional footprint to account for pin connections. The actual board space required depends greatly on the type of connectors used to implement the DP1 daisy chain. For the moment, let us assume the connectors fit within a 20 mm $\times$ 20 mm footprint.[1] Then we can imagine arranging connectors as shown in Figure 4. In this scheme, the required board area is approximately 9 times the FPGA footprint, or 3600 mm^2 per FPGA.

[1]For reference, an RJ-45 ethernet connector includes 8 conductors and requires about 20 mm $\times$ 15 mm; increased density can certainly be achieved.

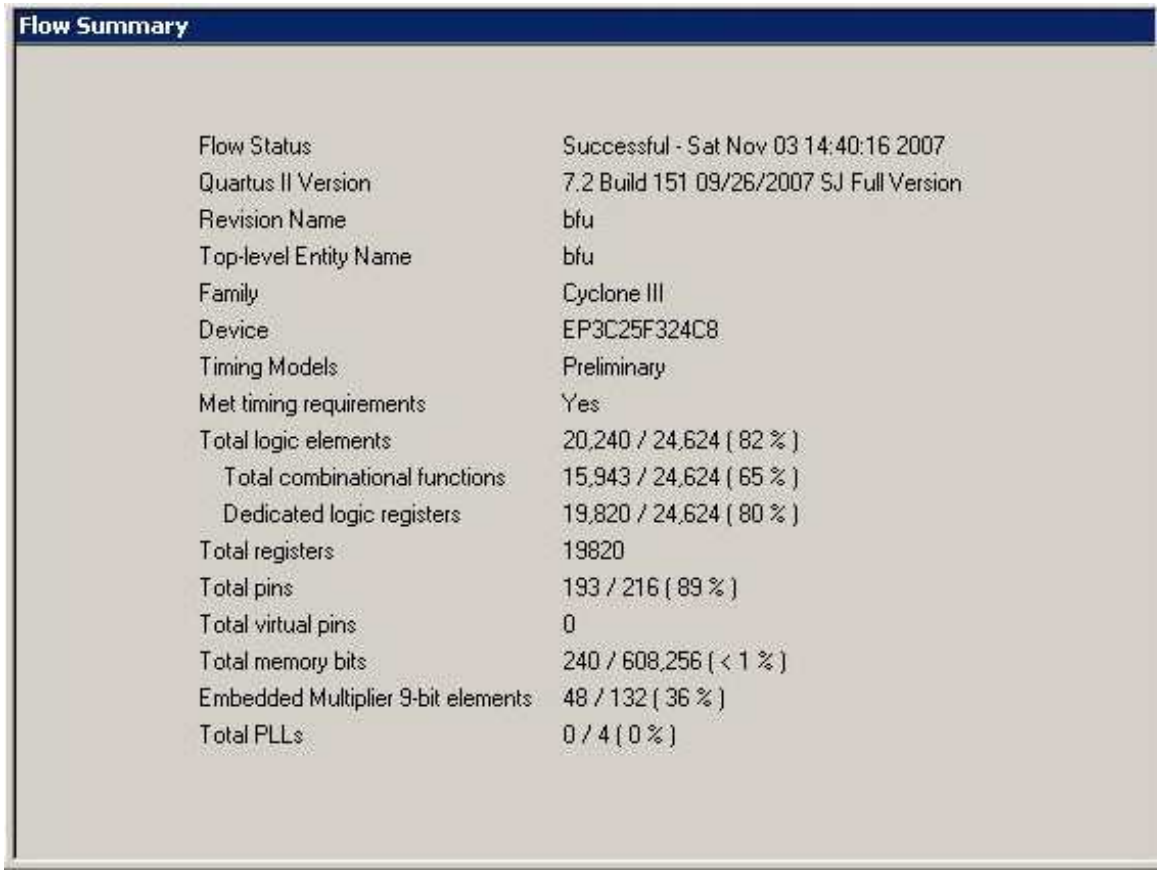

Figure 3: Summary of the design/synthesis flow summary (screenshot from the design software).

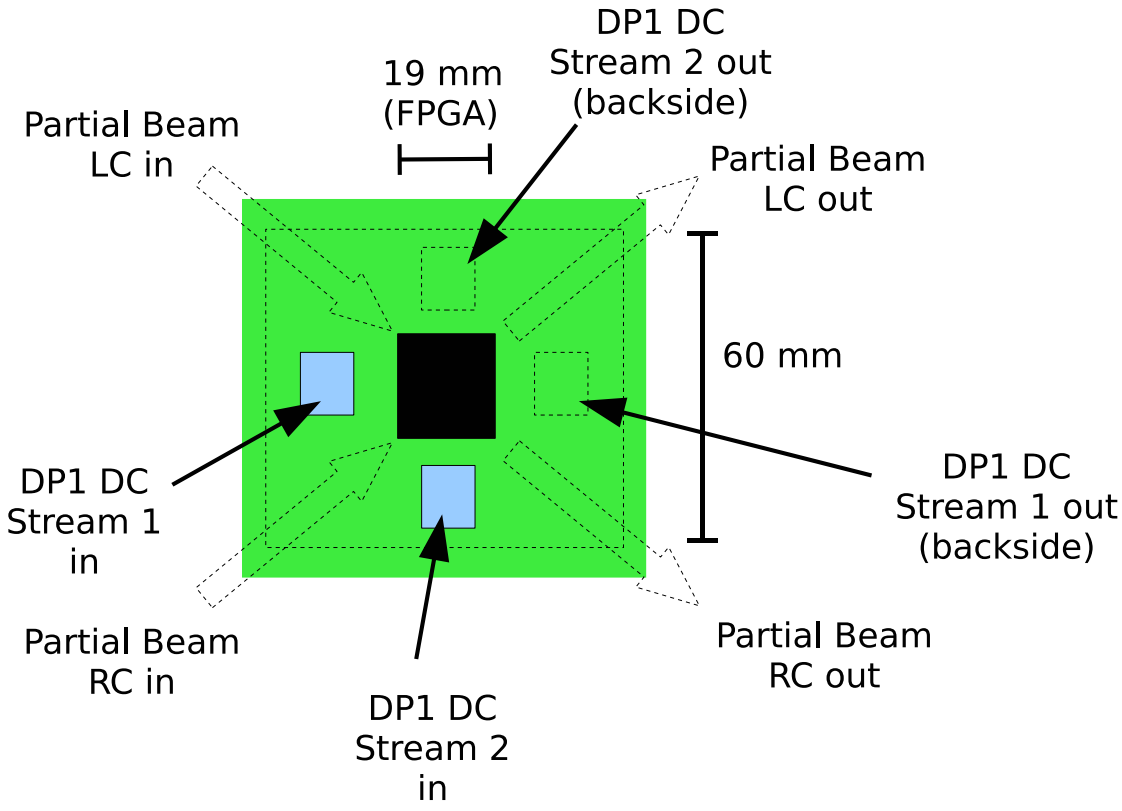

Figure 4: Possible arrangement of FPGAs and connectors. This is a zoomed-in diagram showing the region around one FPGA; the pattern would be repeated over the board as shown in Figure 5. The partial beam signals are traces within the circuit board, directly connecting adjacent FPGAs. Approximately to scale.

A board containing 32 FPGAs arranged in this manner therefore requires about 115,200 mm^2, which corresponds to a square board about 34 cm on a side. Implementing all 128 FPGAs on a single board does not seem reasonable; thus we tentatively take 32 FPGAs/board as a design choice. A possible geometry for such a board is shown in Figure 5. Such a board would fit easily in a standard 19-in rack, which offers about 40 cm usable width, even after allowing additional space for power, control logic, mounting and test points, and so on. It may turn out to be economical to further divide the 40 cm × 40 cm boards into 2 40 cm × 20 cm boards or 4 20 cm × 20 cm boards; in this case, edge connectors could be used to mate the boards into the desired 40 cm × 40 cm 64-stand board shown in Figure 5.

A BFU requires 4 such boards. The only signal connection between the four boards is the "partial beam" signal in two polarizations, which together requires 2 groups of 4 LVDS lanes following the DP1 daisy chain format. Thus, each board is connected to one other board using 8 LVDS lanes. Each such connection can be implemented as a compact cable assembly or ribbon cable consisting of 16 conductors.

The DP1 daisy chain can be implemented without cables by stacking boards and arranging for direct (cable-free) connections between boards. Physically, then, BFUs and other DP1 level-2 subsystems would be interleaved as shown in Figure 6. Note that this scheme requires two very similar but subtly different designs for the boards of the odd-numbered vs. even-numbered BFUs, since the output connectors of the former must connect to the input connectors of the latter.

It is assumed here that 128 channels of DIG subsystems in this scheme can be implemented in the same form factor as the 32-FPGA (64-stand) BFU board. However, following the DIG implementation scheme described in [2] it may not be possible to fit 128 digitizer channels onto a single 40 cm × 40 cm board. Thus, each 128-channel DIG "array" might itself require multiple boards. Alternatively, the DIG boards shown in Figure 6 might be implemented simply as an interface between the BFU boards and digitizers located elsewhere.

Neglecting DIGs for the moment, a DP1 subsystem consisting of 3 BFUs would require 12 boards of about 40 cm × 40 cm. Assuming all boards are arranged in a single stack with 20 mm spacing, the height of the stack is 24 cm. Assuming a height of 40 cm should leave ample space for DIGs and additional hardware required to complete the DP1 chassis. Thus, it appears feasible to implement the DP1 in the space provided by 40 cm (roughly 11U) of vertical space in a standard 19-in rack. Being very conservative to account for mechanical design challenges including thermal control, an entire rack should be set aside for DP1 until more details are worked out.

An alternative method for arranging the boards shown in Figure 6 is to have each stack of four boards, with a DIG board on top, mounted such that the DIG board faces out, forming the front panel of the rack. The remaining three stacks are similarly mounted, forming a front panel roughly 160 cm high by 40 cm wide. The DIG boards then become their own jack panel; analog cables from the ARXs connect directly to DIG boards.

A rough guess at the cost of a single BFU is determined as follows: The cost of the FPGAs is $6400, as mentioned above. A rough guess at the cost of connectors for the daily chain is $10–$20 each, and since there are 4 per FPGA this is $5120–$10,240. A rough guess at the cost of each circuit board, including auxiliary components and assembly, is $2000-$4000 each in small quantities. Taken together, this is $19,520-$32,640 for a single BFU.

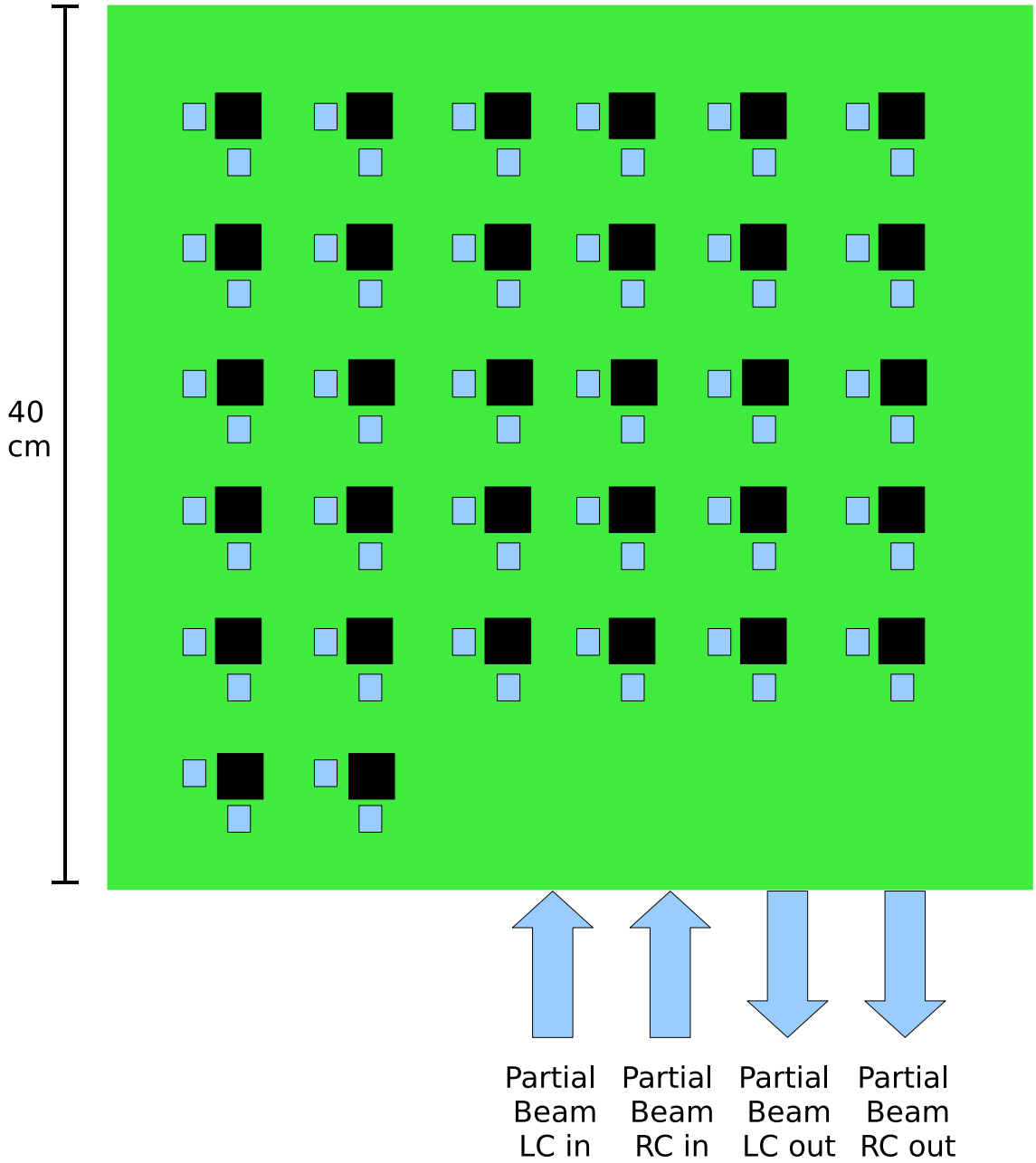

Figure 5: Possible arrangement of FPGAs and connectors to make a board. Approximately to scale. A BFU would consist of 4 such boards.

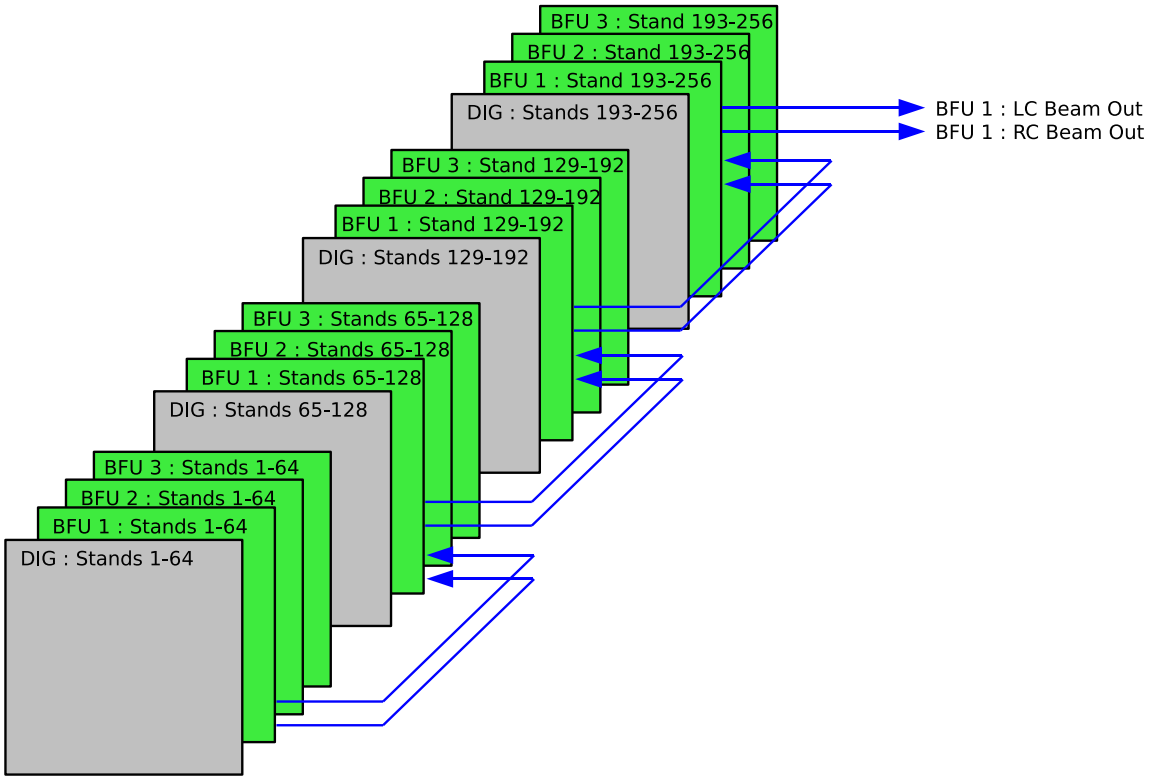

Figure 6: Possible arrangement of boards (as conceived in Figure 5) to form a DP1 subsystem consisting of 3 complete BFUs. "Partial beam" path shown for one BFU (BFU 1) only. See text for an alternative arrangement of the four 64-stand board-stacks.

5 Issues to Address in Future Versions of this Document

1. The requirements for frequency-dependent polarization conversion/calibration need to be worked out and accounted for here.

2. Candidate connectors for implementing the DP1 daisy chain should be identified.

3. Implementation of the DIG will impact electromechanical issues for the BFU, so the DIG should be worked out in the context of the electromechanical design concept presented in this document.

4. Repeat Cyclone III synthesis including actual polarization requirements, FIFO filter, sync/format functionality, LVDS pins, etc.

6 Document History

- This is Version 0.1, which is the first version released.

References

[1] S. Ellingson, "LWA Station Architecture Ver 0.6," October 9, 2007.

[2] S. Ellingson, "ADC Sample Rate and Preliminary Design for a Full-RF ADC Post-Processor," LWA Memo 101, September 11, 2007.

[3] S. Ellingson, "DP1 Daisy Chain Preliminary Interface Control Document Ver. 0.1," Sep 18, 2007. Online: http://www.ece.vt.edu/swe/lwav/.

[4] S.W. Ellingson, "LWA Beamforming Design Concept," LWA Memo 107, October 30, 2007.

[5] S.W. Ellingson, "Polarization Processing for LWA Stations," October 29, 2007.

[6] Altera, Inc., *Cyclone III Device Handbook*, July 2007. This is a two volume set: Currently Vol. 1 is in Version 1.1, Vol. 2 is in Version 1.3. http://www.altera.com.