ADC Selection

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This report documents the selection of analog-to-digital converters (ADCs) for further consideration in LWA. LWA will use a direct sampling scheme which requires digitization at a rate greater than 200 MSPS in order for the entire tuning range (possibly as large as 10-88 MHz according to current planning) to be included comfortably within the first Nyquist zone [1]. ADC requirements for direct-sampling receivers generally are discussed in [2].

A market survey of ADCs has recently been conducted by ARL:UT, which culminated in a recommendation of 6 ADCs for further consideration [3]. One of these (Linear Technology LTC2241-10) was included as one of the six because an evaluation board had been provided at no cost by the vendor; however, based on its specifications it would not otherwise have been recommended and has therefore been excluded from the study reported here. Four parts considered candidates in the ARL:UT study, but not recommended in the "final six", were added to the list considered here. These were the Analog Devices AD9430-210, AD9230-250, AD9230-210, and AD9480. This was motivated by the author's multiple successful past experiences with high-performance ADCs by Analog Devices, and subsequent high level of confidence in this vendor.

The attached table summarizes the evaluation and results. ADCs considered were sorted first by SNR at 80 MHz, and second by SFDR at 80 MHz; in both cases using values reported in manufacturers' datasheets via [3]. The top-performing candidate after this sort – TI's ADS5474 – was excluded because the #2 candidate – Maxim's MAX1215N – appears to perform nearly as well but with greatly reduced power consumption and much lower cost. Candidates #3 and #4 were similarly excluded because the #5 candidate, the Analog Devices AD9230-250, performed nearly as well with greatly reduced power consumption. The National ADC08200 is unacceptable for a number of reasons, including low SNR, single-ended interfaces, and CMOS outputs – all quite risky considering the application and likely design requirements.

The conclusions are as follows:

(1) The Maxim MAX1215N appears to be best overall choice.

(2) The Analog Devices AD9211-300 is a very strong contender, and should be evaluated side-by-side the MAX1215N. Although SNR and SFDR are considerably less than those of the MAX1215N, these specifications appear to be fully satisfactory from the perspective of requirements as we currently understand them, and are obtained at an impressively high sample rate of 300 MSPS (in contrast to 250 MSPS for the MAX1215N). The reported typical power consumption of 437 mW is about one-half that of the MAX1215N, and this is large enough that it could end up being a significant fraction of the per-antenna station power consumption. The AD9211-300 costs about half that of the MAX1215N (possibly, but not likely to be a significant factor overall), and includes a built-in test pattern generation feature which is likely to be useful in development and system-level diagnostics.

(3) The Analog Devices AD9230-250 and -210 should be considered as tertiary alternatives, but not necessarily evaluated.

(4) In the event of extreme cost pressure, the Analog Devices AD9480 may provide an acceptable alternative, but should not necessarily be evaluated. In this case, cost reduction by a factor of about 3 is obtained at the expense of specifications which just barely meet requirements, as best as we understand them currently.

Availability has been investigated for the MAX1215N and AD9211-300. While availability of high-performance ADCs over long periods is always a bit of a gamble, no specific cause for concern was noted in either case. Both parts are currently available in both large and small quantities with lead times less than 2 months.

References

[1] S. Ellingson, "LWA Station Architecture Ver 0.5," August 28, 2007.
[2] D.W.A. Taylor III, *Design of Ultrawideband Digitizing Receivers for the VHF Low Band,* Masters Thesis, Virginia Polytechnic Institute & State University, 2006. http://scholar.lib.vt.edu/theses/available/etd-05162006-161217/.
[3] J. York, V. Sitaram, and L. Shuhatovich, "LWA ADC Candidate Selection DRAFT v0.2," 8/23/07.

A/D Evaluation Study
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SORT PRIORITY ==>									**1**	**2**		
Mfr	*Part No*	*Selected in ARL Study?(1)*	*# input chan*	*MSPS*	*bits*	*$ (1K)*	*Output Format*	*Typ Pwr [mW]*	*SNR 80 MHz [dB]*	*SFDR 80 MHz [dB]*	*Eval. Priority*	*comments*
TI	ADS5474	YES	1	400	14	$150.00	LVDS	2500	69	85		Exclude -- can do nearly as well with MAX1215N at much lower power & cost
Maxim	**MAX1215N**	**YES**	**1**	**250**	**12**	**$89.50**	**LVDS**	**886**	**67**	**85**	**1**	**SELECT: This looks really good.**
TI	ADS5463	YES	1	500	12	$125.00	LVDS	2250	64	83		Exclude -- can do nearly as well with AD9230-210/250 at much lower power & cost
ADI	AD9430-210	no	1	210	12	$55.00	LVDS	1500	64	82		Exclude -- can do nearly as well with AD9230-210/250 at much lower power & cost
ADI	**AD9230-250**	**no**	**1**	**250**	**12**	**$59.00**	**LVDS**	**434**	**64**	**78**	**3**	**SELECT: Almost as good as MAX1215N at significantly lower cost & power**
ADI	AD9230-210	no	1	210	12	$42.00	LVDS	383	64	78	4	[SELECT as alternate to -250 version if sample rate permits]
ADI	**AD9211-300**	**YES**	**1**	**300**	**10**	**$46.00**	**LVDS**	**437**	**59**	**80**	**2**	**SELECT: Competitive with AD9230, allows higher clock rate, BIT pattern generator feature**
ADI	AD9480	no	1	250	8	$16.00	LVDS	439	47	68	5	Exclude(2) -- Not competive in terms of SNR or SFDR
National S	ADC08200	YES	1	200	8	$7.67	CMOS	210	45	56		Unacceptable -- SNR too low, SFDR very poor. Also, single-ended clock, CMOS outputs…

Notes

(1) York, Sitaram, and Shuhatovich, "LWA ADC Candidate Selection DRAFT v0.2", 8/23/07
(2) Revisit this choices if ADC cost appears to become a constraint, as cost is dramatically less
(3) Typ pwr, SNR, and SFDR specs taken from ARL study (see (1))