MCS Architecture
Ver. 4

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Contents

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1 Architecture

MCS stands for "monitoring and control system". MCS is defined in [1]. The purpose of this document is to describe the architecture of MCS (not discussed in [1]) and to provide the next lower level of design detail.

Figure 1 shows the MCS architecture, as well as interfaces to adjacent subsystems. First, note that here we use the term "MCS" to refer to both MCS (the upper shaded region) as well as the MCS Data Recorder ("MCS-DR"; the lower shaded region). Excluding MCS-DR for the moment, note that MCS consists of three computers and two switches. These are described below:

- The *Scheduler* is a computer whose primary function is to issue commands and receive status from other LWA subsystems. The command and status communications are though the *Command Hub*, using the "MCS Common ICD" [2] augmented by the corresponding subsystem ICDs. The term "scheduler" is a bit of a misnomer, since it does not actually do scheduling, but rather keeps time, issues commands necessary to implement instructions from the Executive, parses the stream of incoming response messages. The Scheduler manages the Command Hub. The Scheduler handles tasks that are extremely time-sensitive and that must be coordinated on timescales down to milliseconds.

- The *Executive* is the computer which exercises top-level control over MCS as well as the station. It is responsible for interpreting observation requests and, from these, generating the data which becomes the content of command messages issued by the Scheduler. This includes numerically-intensive operations such as computation of FIR filter coefficients. It updates the MCS and station MIBs accordingly. The Executive manages the Gateway. The Executive manages tasks that are moderately time-sensitive and that must be coordinated on timescales down to seconds.

- The *Task Processor* is a computer which exists primarily to host applications which are not "time critical" and therefore can be "offloaded" to reduce the processing burden of the Executive. The Task Processor is the primary interface with users, managing command line and GUI interactions. Prominent among these are observation scheduling, including the reduction of scheduled observation data from "user friendly" form to parameterized instructions that can be interpreted by the Executive. The Task Processor is also responsible for the scheduling and interpretation of internal diagnostics (both automatic or user-directed), and manages MCS-DR. In general, the Task Processor handles tasks that do not need to managed at resolutions of seconds or less.

- The *Gateway* is a managed switch which, under the control of the Executive, regulates the flow of network traffic between the Shelter LAN and the various computers of MCS and MCS-DR. The Gateway is managed to prevent traffic from the Shelter LAN from interfering with MCS operation, as well as to provide a layer of security between the shelter LAN (and external network) and MCS-internal devices. The Gateway is also used to regulate the flow of data between the MCS-DR computers and users who are retrieving data or otherwise utilizing MCS-DR computers.

- The *Command Hub* is a managed switch which, under the control of the Scheduler, regulates the flow of network traffic between the Scheduler and subsystems, utilizing the "MCS Common ICD" interface [2]. The Command Hub is managed in order to guarantee sufficient allocation of bandwidth between connected devices, and to avoid any connected devices from interfering with MCS operation by "jabbering" or exhibiting other problematic behaviors beyond the control of MCS.

MCS-DR consists of 5 identical computers as shown in Figure 1. Four of these computers receive data streams from DP corresponding to the output of each of the four station beams. The fifth computer receives the DP output data stream corresponding to TBW/TBN output. Each MCS-DR

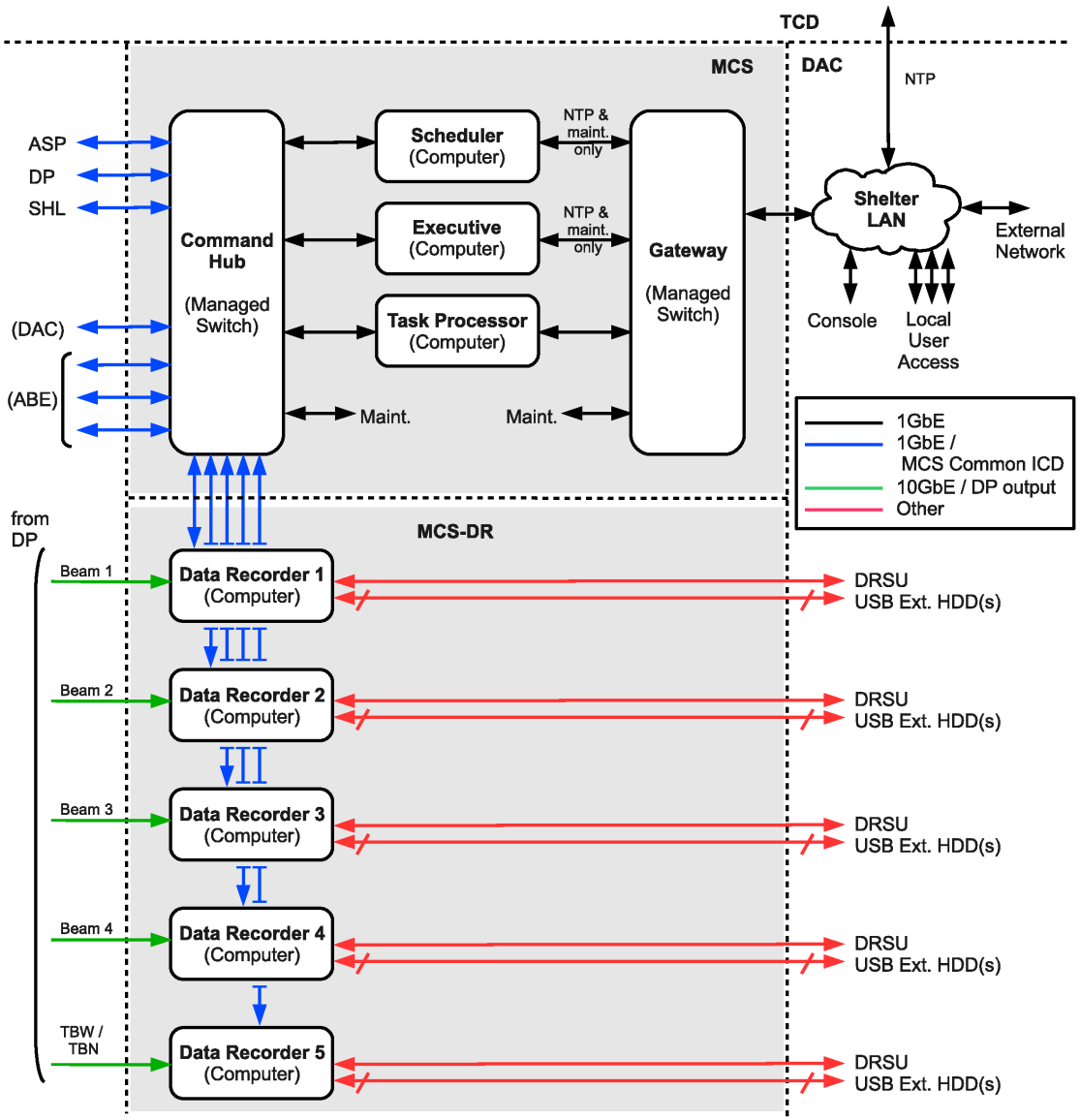

Figure 1: MCS architecture and interfaces to adjacent subsystems. "DAC" refers to "Data Aggregation and Communications" (not currently implemented in LWA-1). "ABE" refers to "alternative back ends" (not currently defined, but taken into account to facilitate future expansion). "DRSU" refers to "data recorder storage unit" (see text). "Maint." refers to (1) access ports to allow connection of laptop-type computers for development, integration, and troubleshooting activities, and (2) data paths available for the same purposes.

computer is connected to a separate, removable data recorder storage unit ("DRSU"). A DRSU is a hard drive array having total storage of 5TB, connected to an MCS-DR computer via an eSATA cable. All data acquired by an MCS-DR computer is streamed directly to its associated DRSU. For additional information, see [3, 4].

When not being used for data recording, MCS-DR computers are also available for general purpose computing by MCS, or by users (under MCS control). See [1] for additional details on how MCS-DR is to be used.

Note that the shelter LAN and physical access for local users are not part of MCS. (It presumed that these will eventually be subsumed into the DAC subsystem.) Also note that a "console" (that is, a permanently-installed computer for operation of the station by local users) is not part of MCS. For elaboration, please see [1].

2 Document History

- Version 4 (Nov 7, 2009):
  - Revised architecture diagram to remove PPS and 10 MHz interfaces into MCS/Scheduler (determined that NTP will suffice).
  - Revised architecture diagram to replace LTO tape drives with DRSUs.
- Version 3 (Feb 25, 2009):
  - Revised architecture diagram to indicate an "MCS Common ICD" connection to SHL. J. Craig indicates that SHL will have a computer which in turn will control SHL-PCD and SHL-ECS.
- Version 2 (Feb 23, 2009):
  - TBW/TBN input to MCS-DR now indicated as 10 Gb/s.
  - J. Craig indicates that PCD will require an unknown number of "MCS Common ICD" interfaces. These have been added.

References

[1] S. Ellingson, "MCS Subsystem Definition," Ver. 2, Long Wavelength Array Engineering Memo MCS0004, Feb. 23, 2009. [online] http://www.ece.vt.edu/swe/lwavt/.

[2] S. Ellingson, "MCS Common ICD," Ver. 1.0, Long Wavelength Array Engineering Memo MCS0005, Apr 04, 2009. [online] http://www.ece.vt.edu/swe/lwavt/.

[3] C. Wolfe, S. Ellingson & C. Patterson, "Interface Control Document for Monitor and Control System Data Recorder," MCS0020, Oct 10, 2009. [online] http://www.ece.vt.edu/swe/lwavt/.

[4] C. Wolfe, S. Ellingson & C. Patterson, "MCS-DR Storage Unit," MCS0019, Sep 23, 2009. [online] http://www.ece.vt.edu/swe/lwavt/.